Creating Long-Term Customer Value

The Path to IA-64 Systems

www.hp.com/go/ia-64

Next Generation Technology

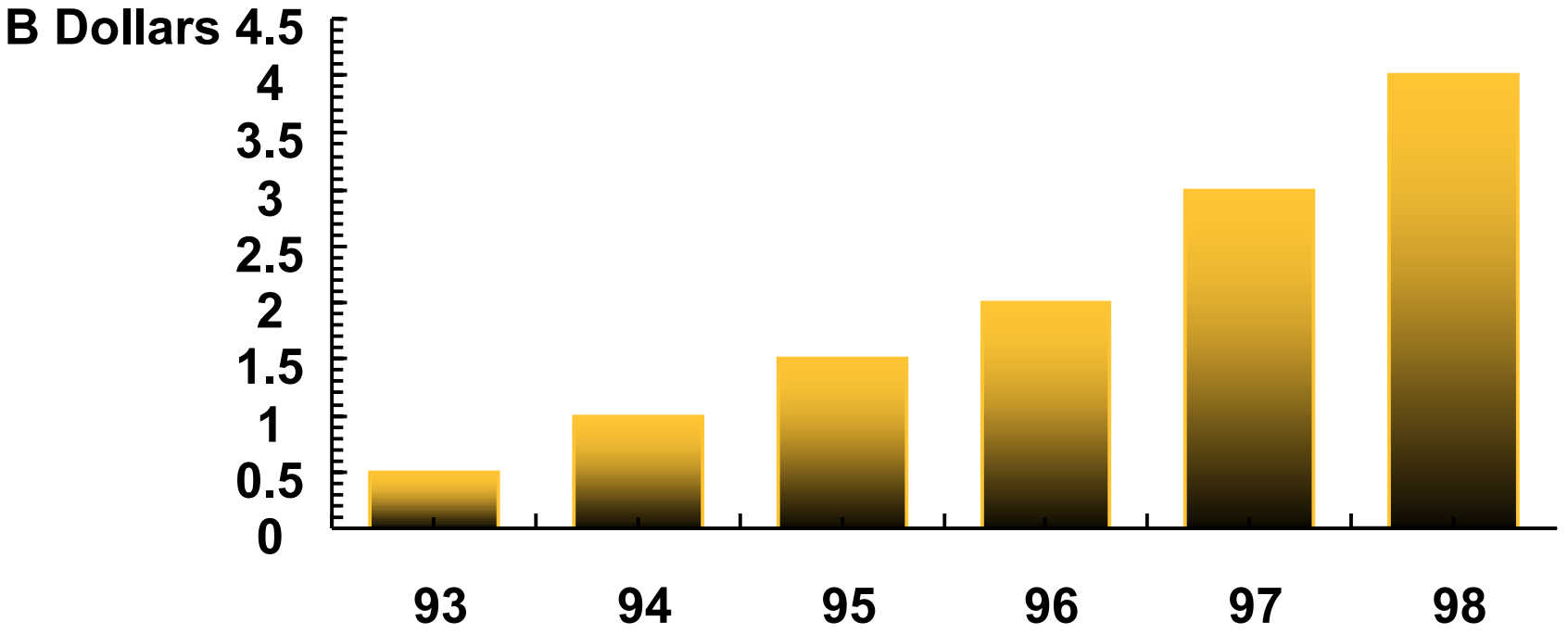
EPIC: The next generation processor technology.
- CISC: Complex Instruction Set Computing
- RISC: Reduced Instruction Set Computing
- **EPIC: Explicitly Parallel Instruction Computing**

IA-64: The architecture that incorporates EPIC technology.
- PA-RISC: Precision Architecture - RISC
- IA-32: Intel Architecture - 32-bit
- **IA-64: Intel Architecture - 64 bit**

Itanium: The first IA-64-based microprocessor from Intel.
- Pentium II processor
- PA-8500
- **Itanium® Processor**

New Fab Costs Accelerating

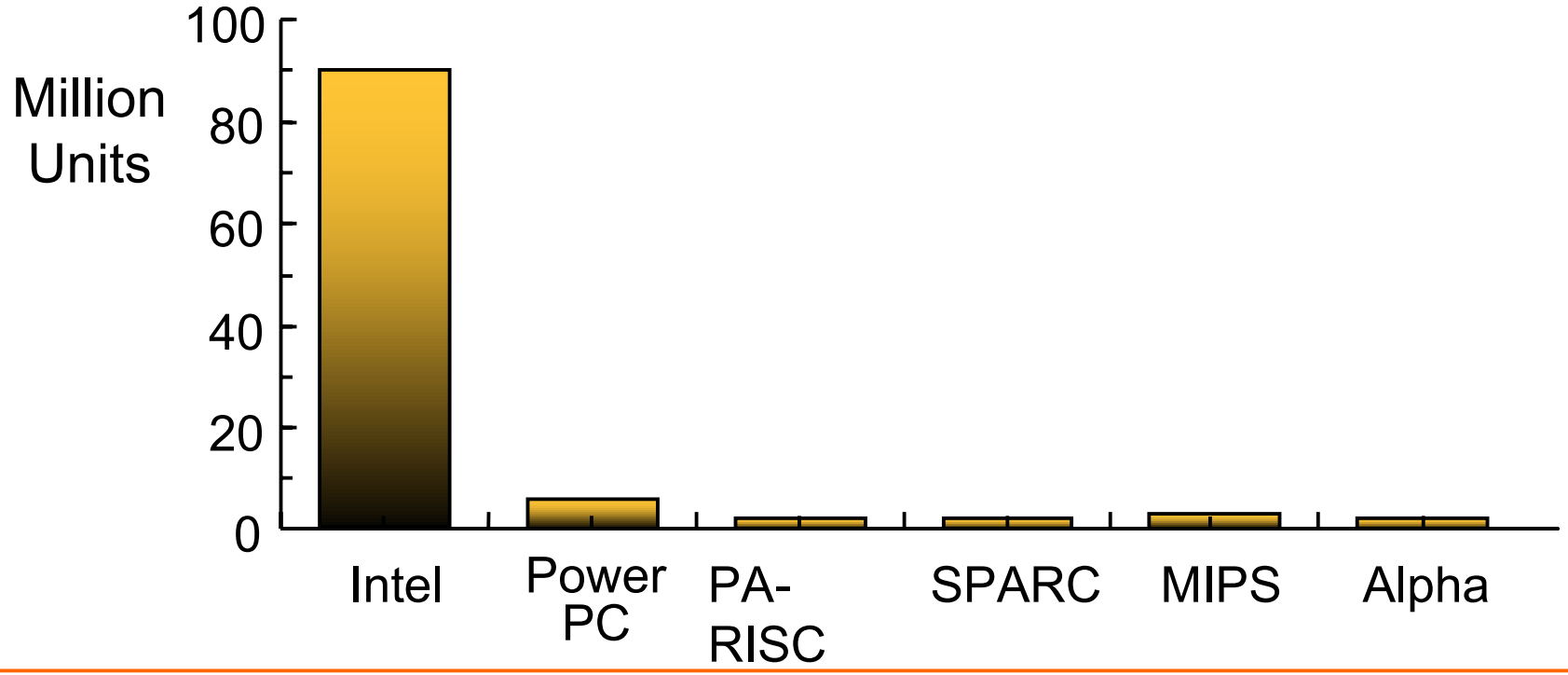
How many proprietary RISC vendors can continue to invest?



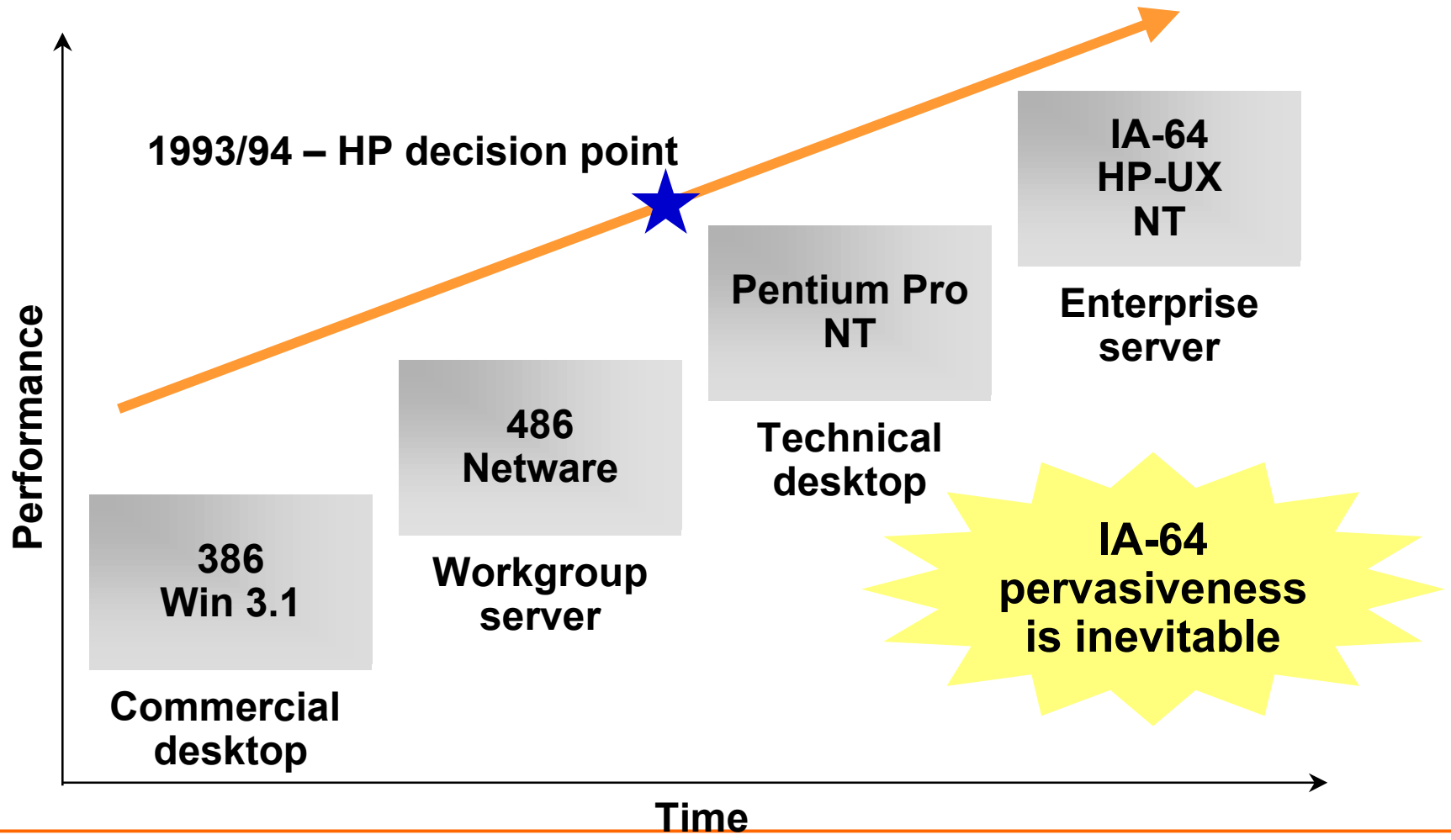
(...or, alternatively, face higher chip COGS, TTM, supply assurance and quality issues if they go with a third party fab?)

Microprocessor Production Capacity

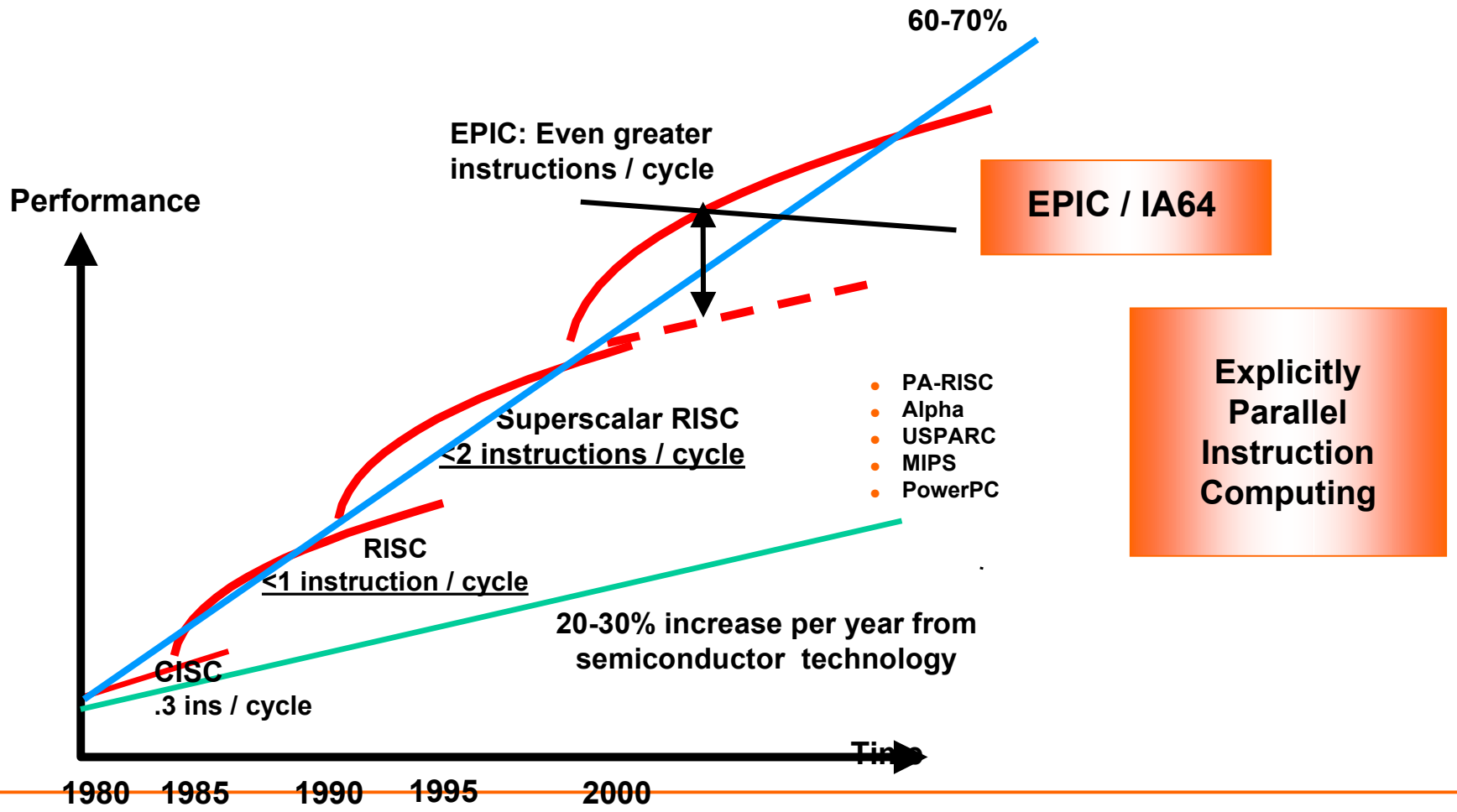
Especially when fabrication and design costs must be recouped against relatively small unit volumes compared with merchants...



The Inevitability of IA-64

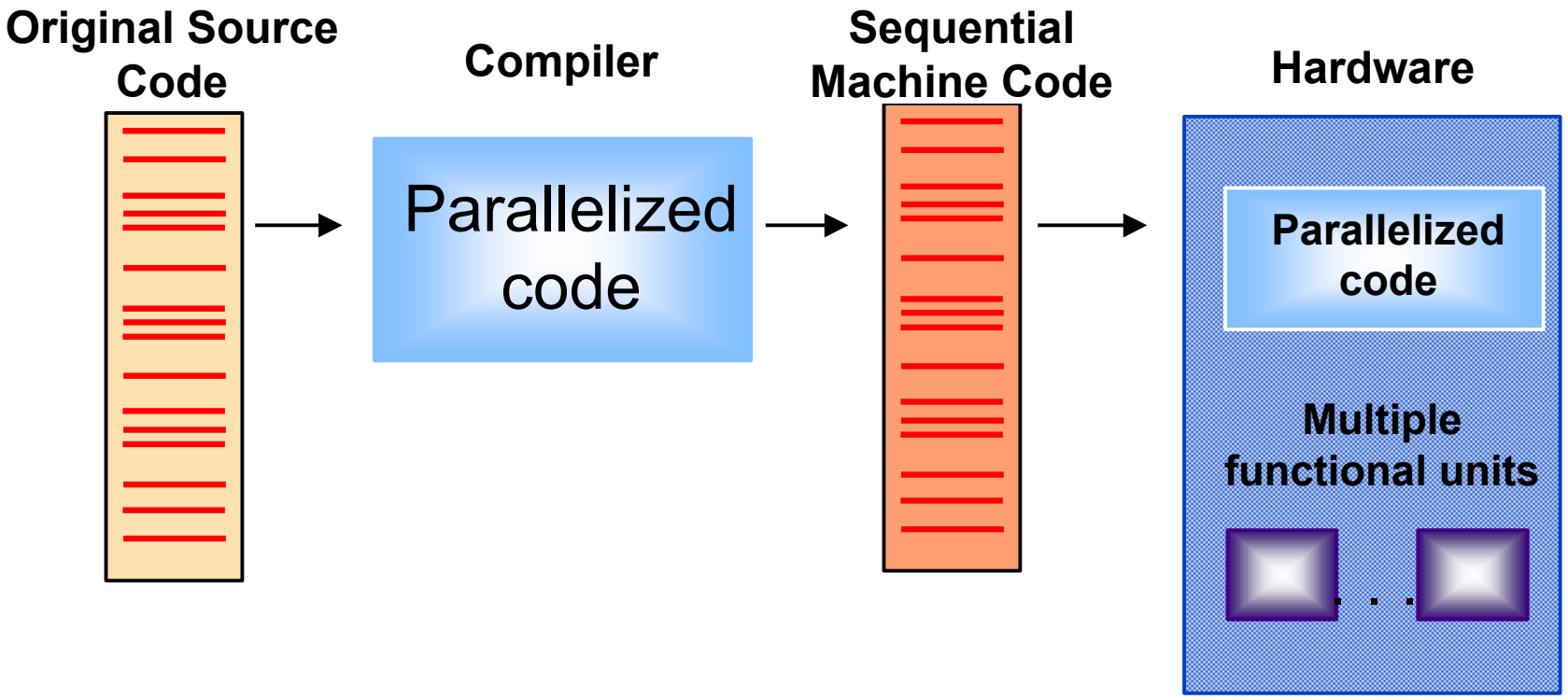


Evolution of Microprocessor Technology



Today's Implementation: Implicit Parallelism

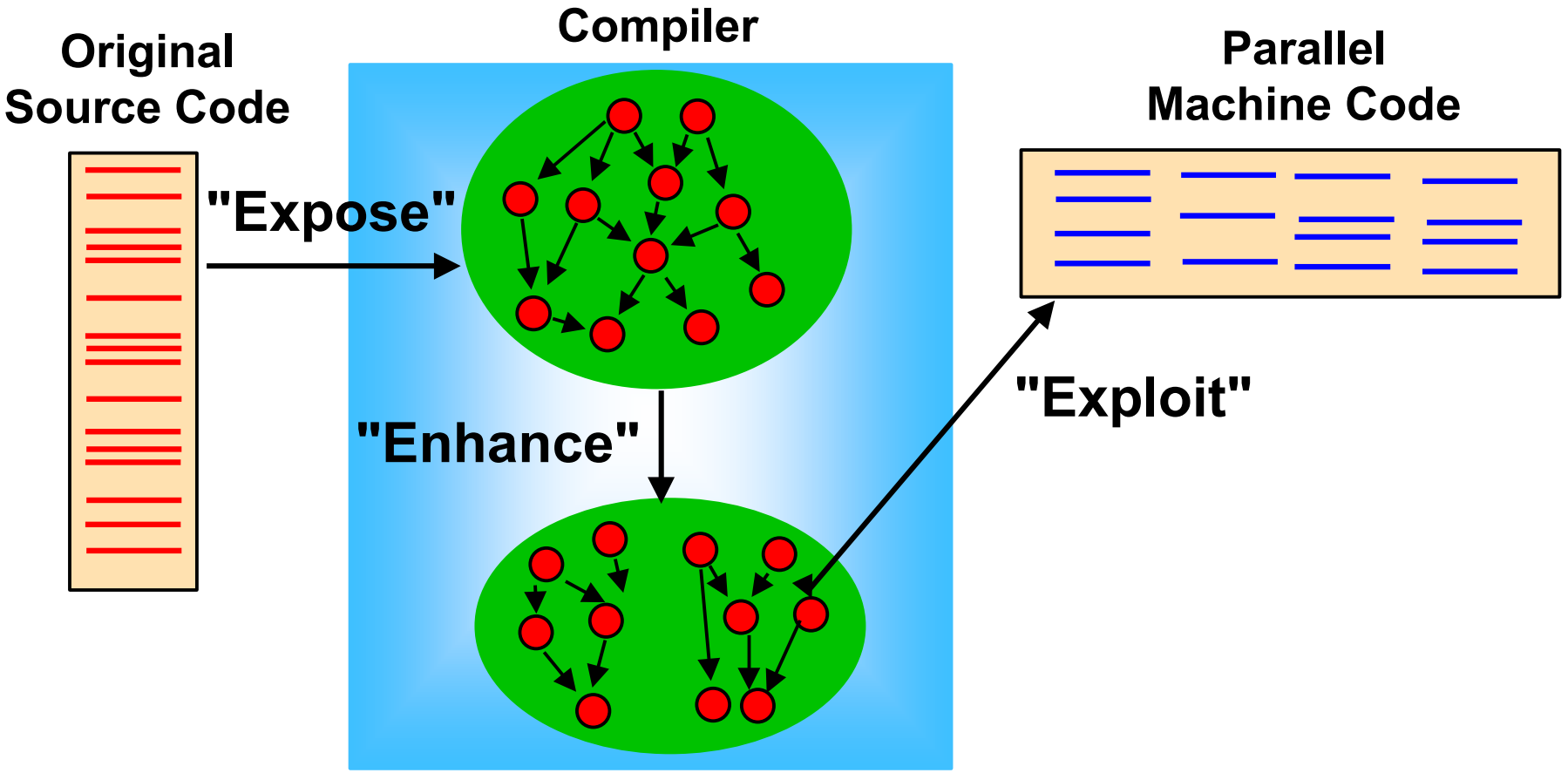
Sequential execution model:



Compiler has a limited, indirect view of hardware, which limits performance

EPIC Model: Explicit Parallelism

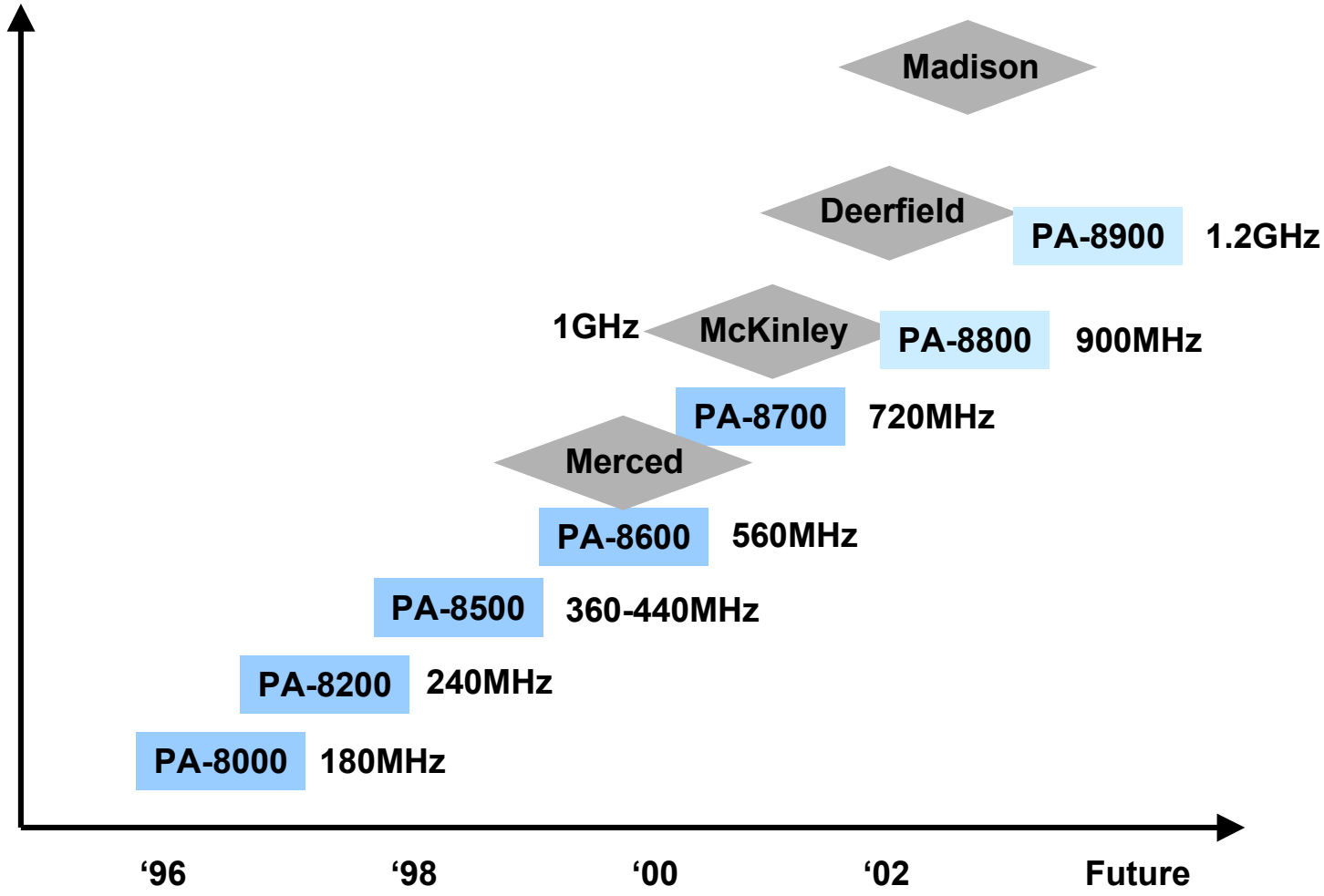
Compiler exposes, enhances and exploits parallelism in the source program and makes it explicit in the machine code



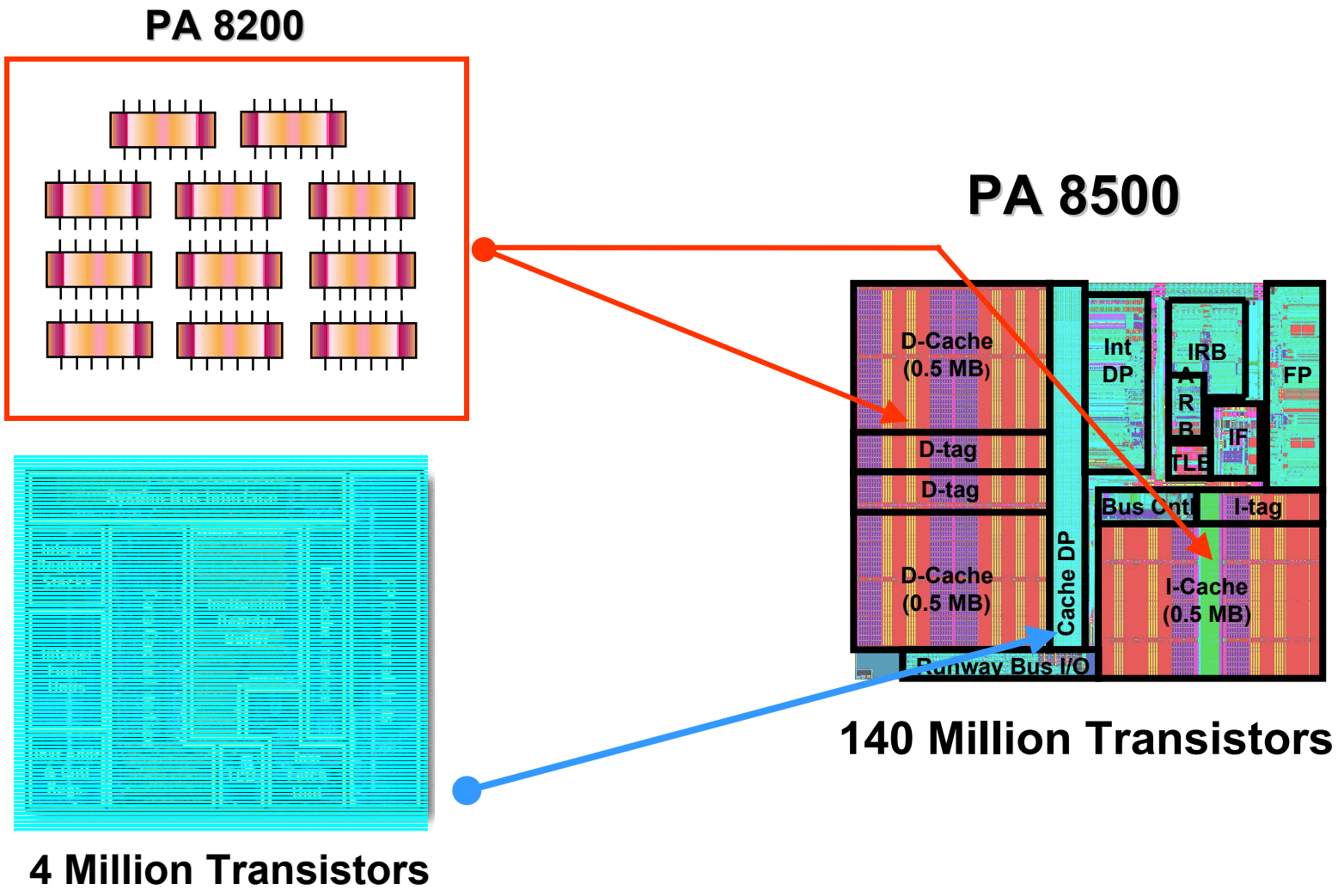
Industry Momentum Behind IA-64

Every major platform but Apple has made a commitment to IA-64

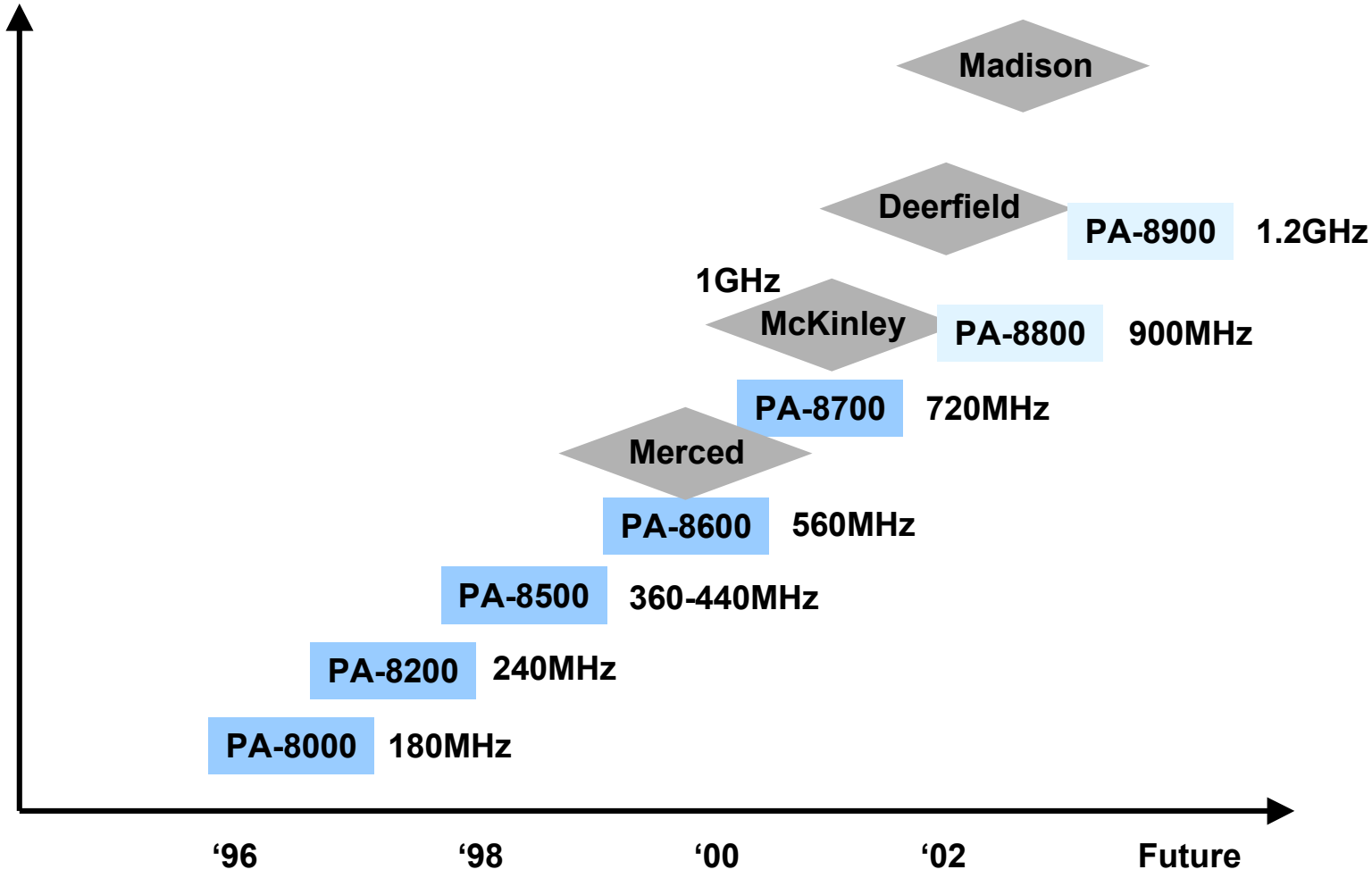
Microprocessor Roadmap



Impact of .25µ Technology

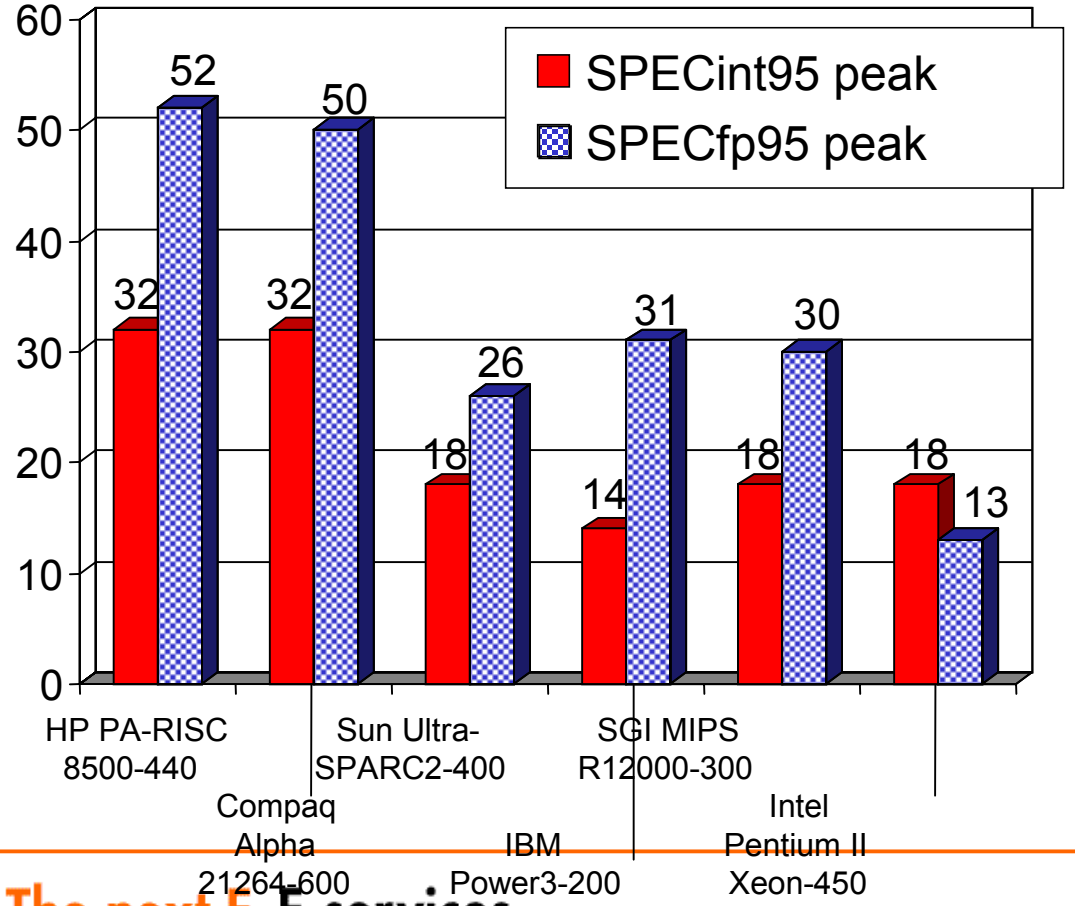


Microprocessor Roadmap



PA-8500 Performance Breakthrough

- Leadership performance
- 1.5MB on-chip cache
- 140 Million transistors
- Improved Branch Prediction



PA-RISC 8500 Base:
Specint95 est: 30
Specfp95 est: 50

PA-RISC 8500 Peak:
Specint95 est: 32
Specfp95 est: 52

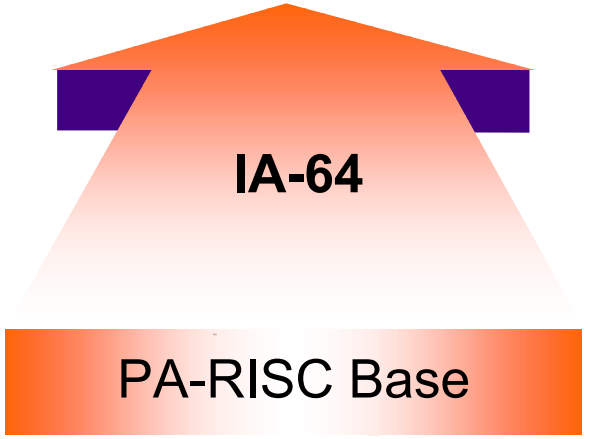
Sources: HP for 8500 and Linley Gwennap (MicroDesign Resources, 10/7/98) for apples-to-apples SPEC comparison numbers

PA-RISC Will Live on Through IA-64

IA-64 retains many key PA-RISC characteristics:

1-to-1 mapping of performance-sensitive machine-level instructions

- PA-RISC virtual memory architecture
- Identical data formats
- PA-RISC floating point (IA-64 is a superset)
- PA-RISC multimedia (IA-64 is a superset)
- PA-RISC graphics acceleration

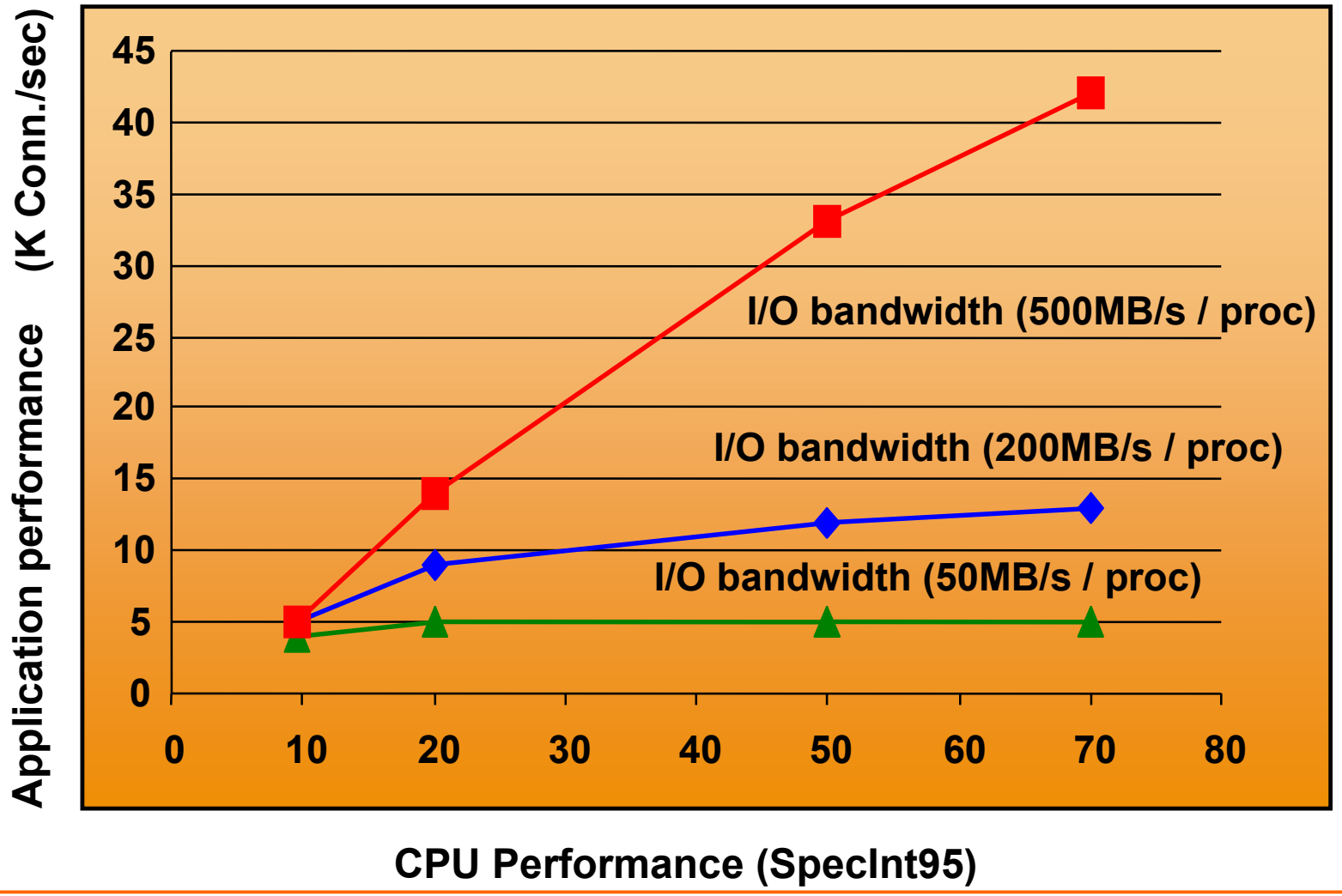


Benefits for PA-RISC customers:

- Smoother transition to IA-64 architecture designed in
- Easier ISV migration means more applications available sooner
- Better performance and reliability--functionality out sooner

Key: avoid "dead ends" where vendor can't move customers forward

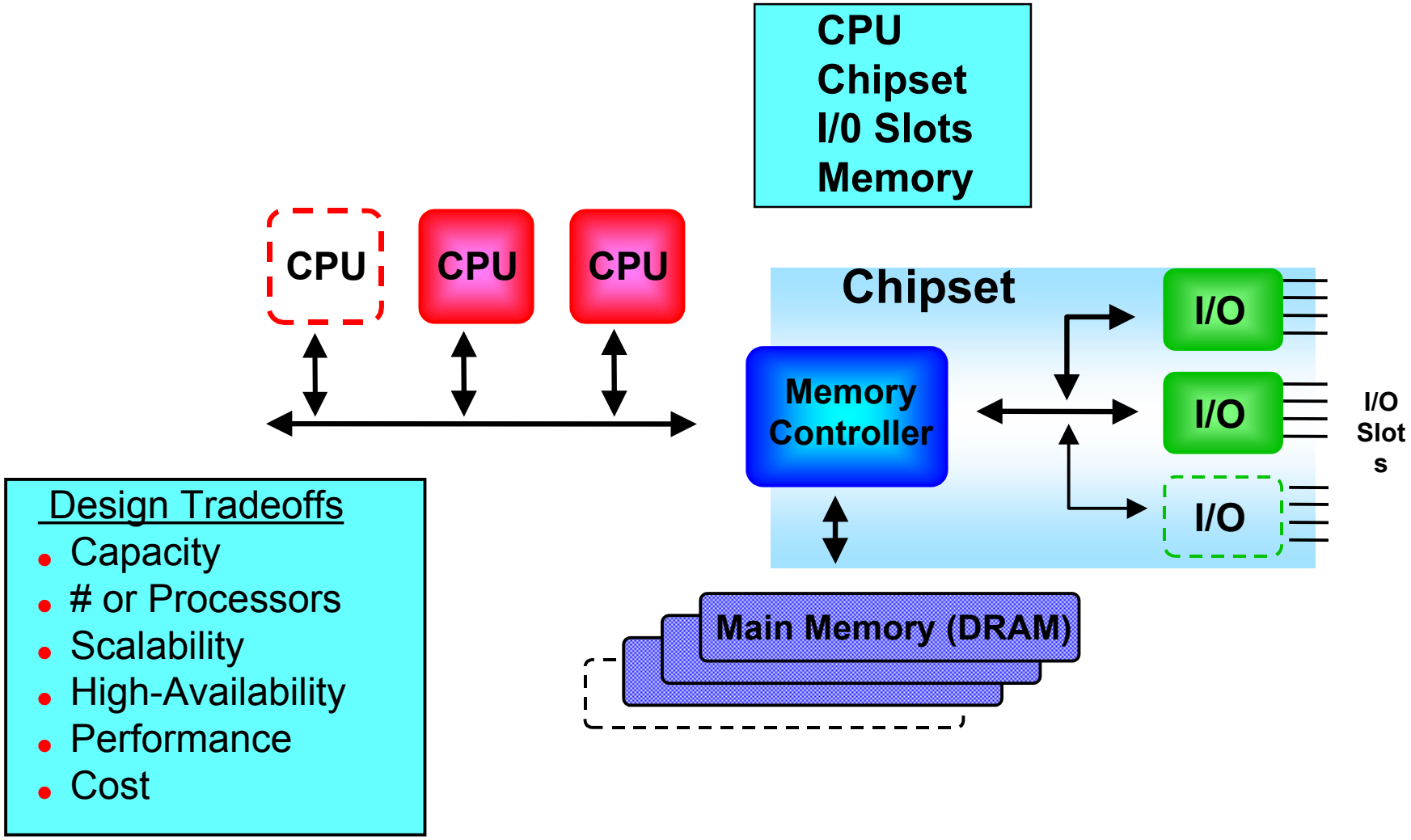
The Requirement for Balanced System Design



Chipset Analogy

- Microprocessor = Automobile Engine
- Chipset = Drive train, suspension, and transmission
- Many automobiles share the same engine and differentiate on drive trains (front wheel, 4 wheel), transmissions (stick, automatic) and suspensions (sport, smooth ride)
- So will computer vendors differentiate with chip sets

System Building Blocks



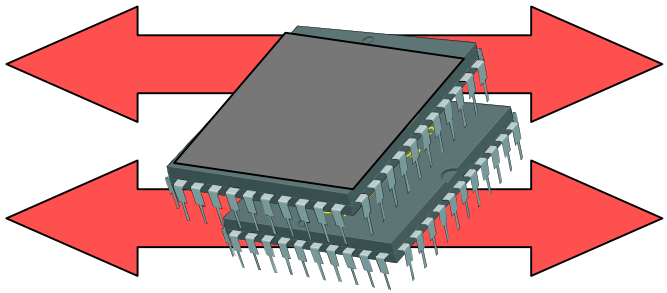
Design Tradeoffs

- Capacity
- # or Processors
- Scalability
- High-Availability
- Performance
- Cost

World's First IA-64 SMP Chipset and Bus

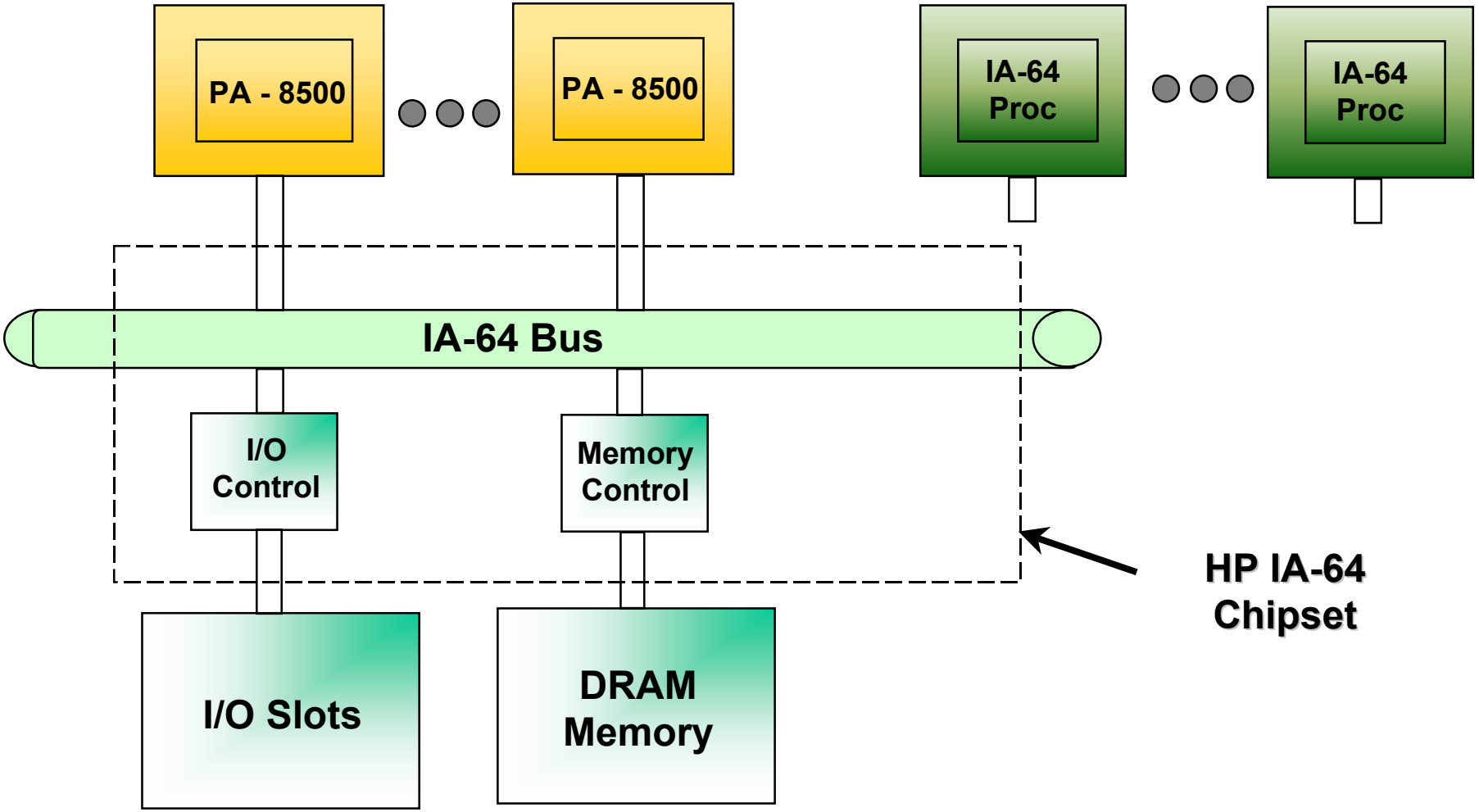
IA-64 system bus will be in HP's 1999 PA-RISC and IA-32 Systems, and in board upgrades with IA-64 processors

- Sustained industry-leading performance
- Excellent multi-bus support and scalability
- Supports "Five 9's" High-Availability initiative
- HP-UX, MPE, NT-32 & NT-64
- PA-RISC, IA-32, IA-64
- Longevity: Investment Protection



This first IA-64 Hardware demo underscores HP's continuing commitment to IA-64 leadership

HP IA-64 Ready System Block Diagram



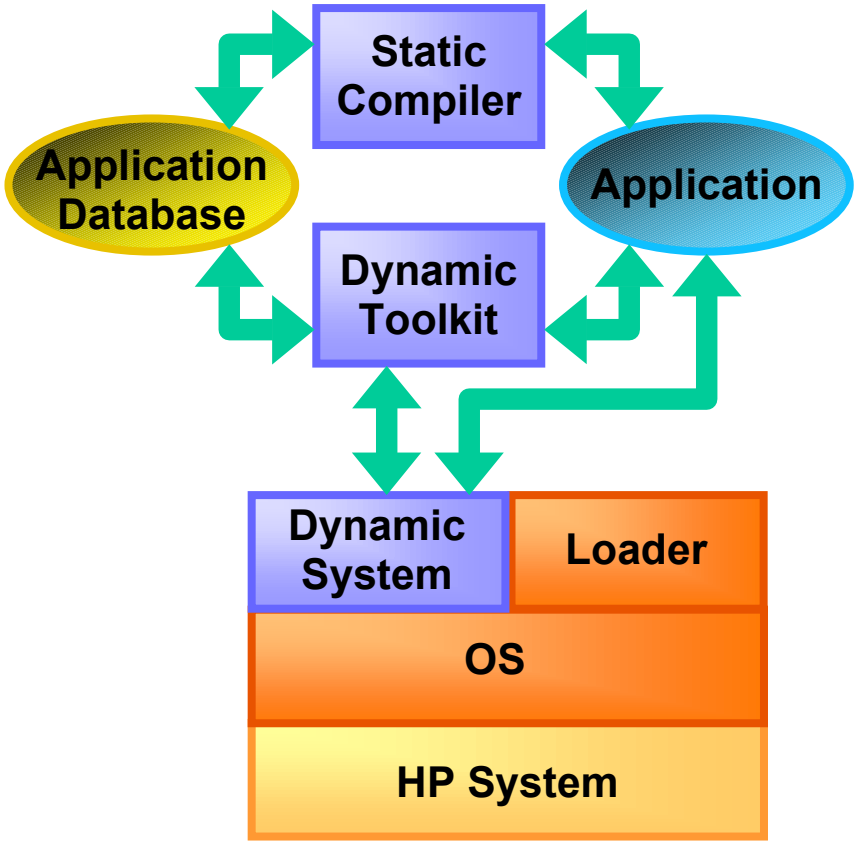
Compiler Analogy

- EPIC is like the TGV from Paris to Lyon: It is capable of consuming miles and miles of track at a very rapid pace.

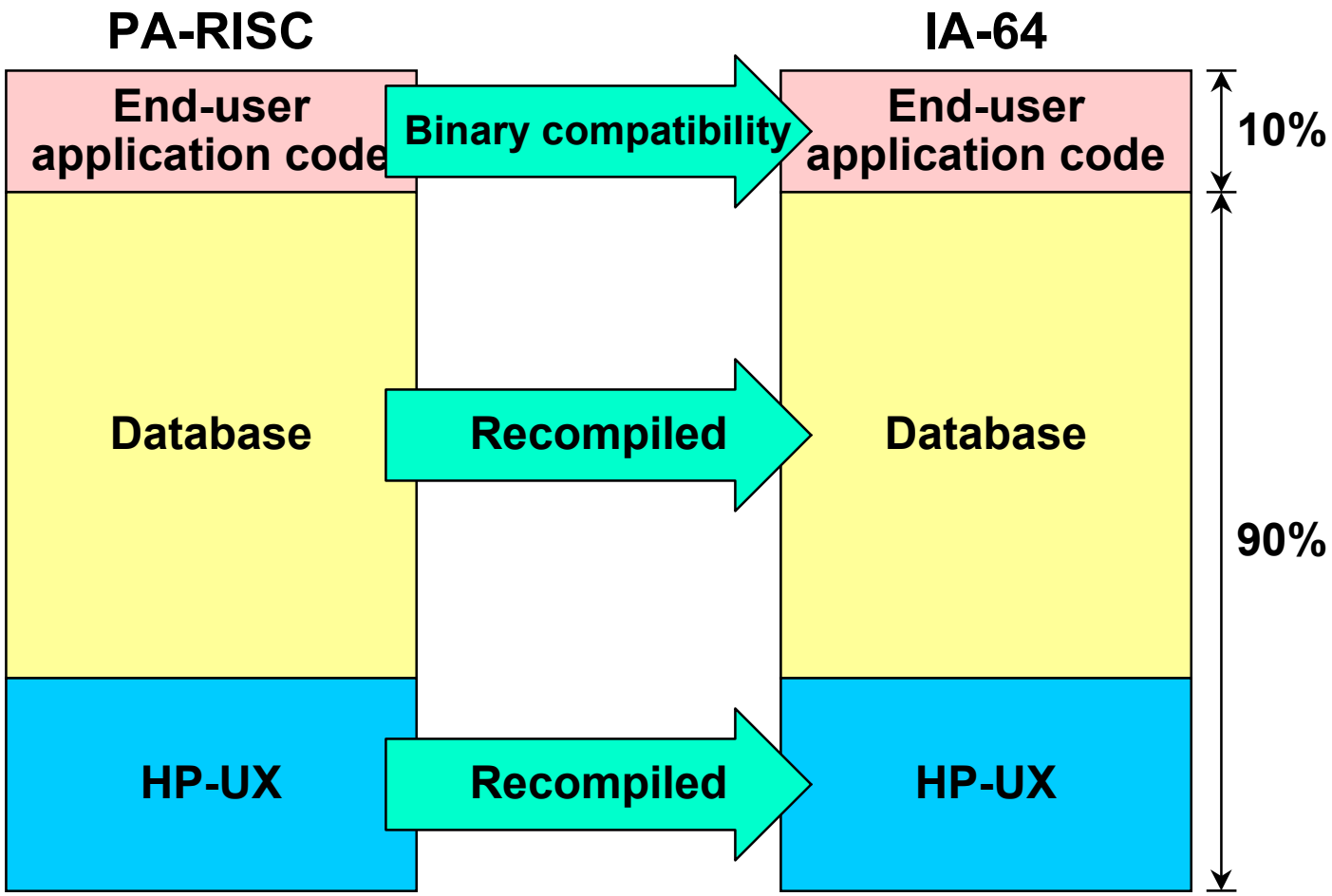
- It is the compiler technology that keeps the train from stopping at the small towns along the way.

High Performance Compiler

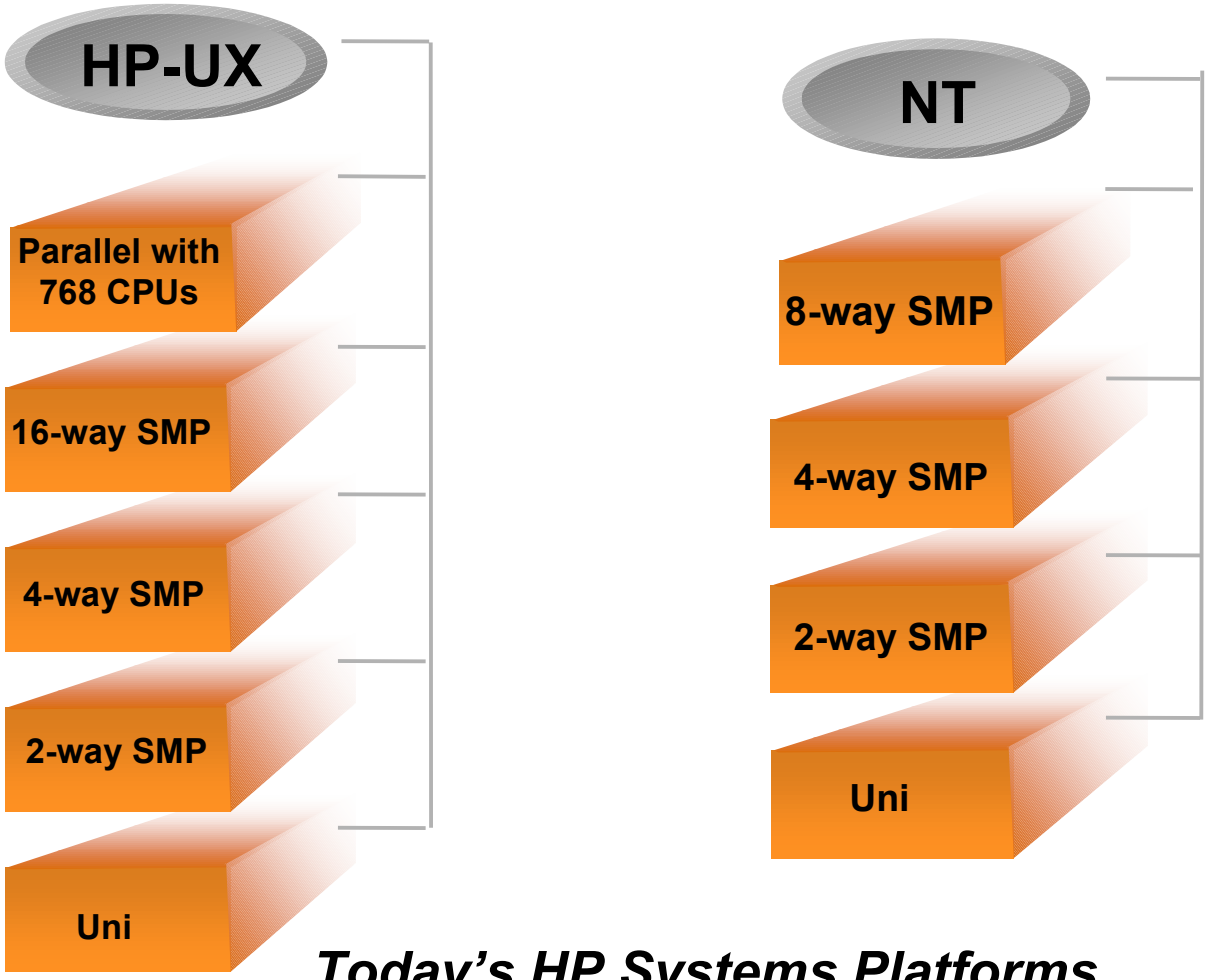
- **Compiler provides critical support for key IA-64 features**
  - Speculation, predication
- **Dynamic Toolkit customizes performance**
  - Analyze program behavior
  - Focus on critical code
- **HP has the experience and expertise**



90% of Performance Gain Comes From HP-UX and RDBMS

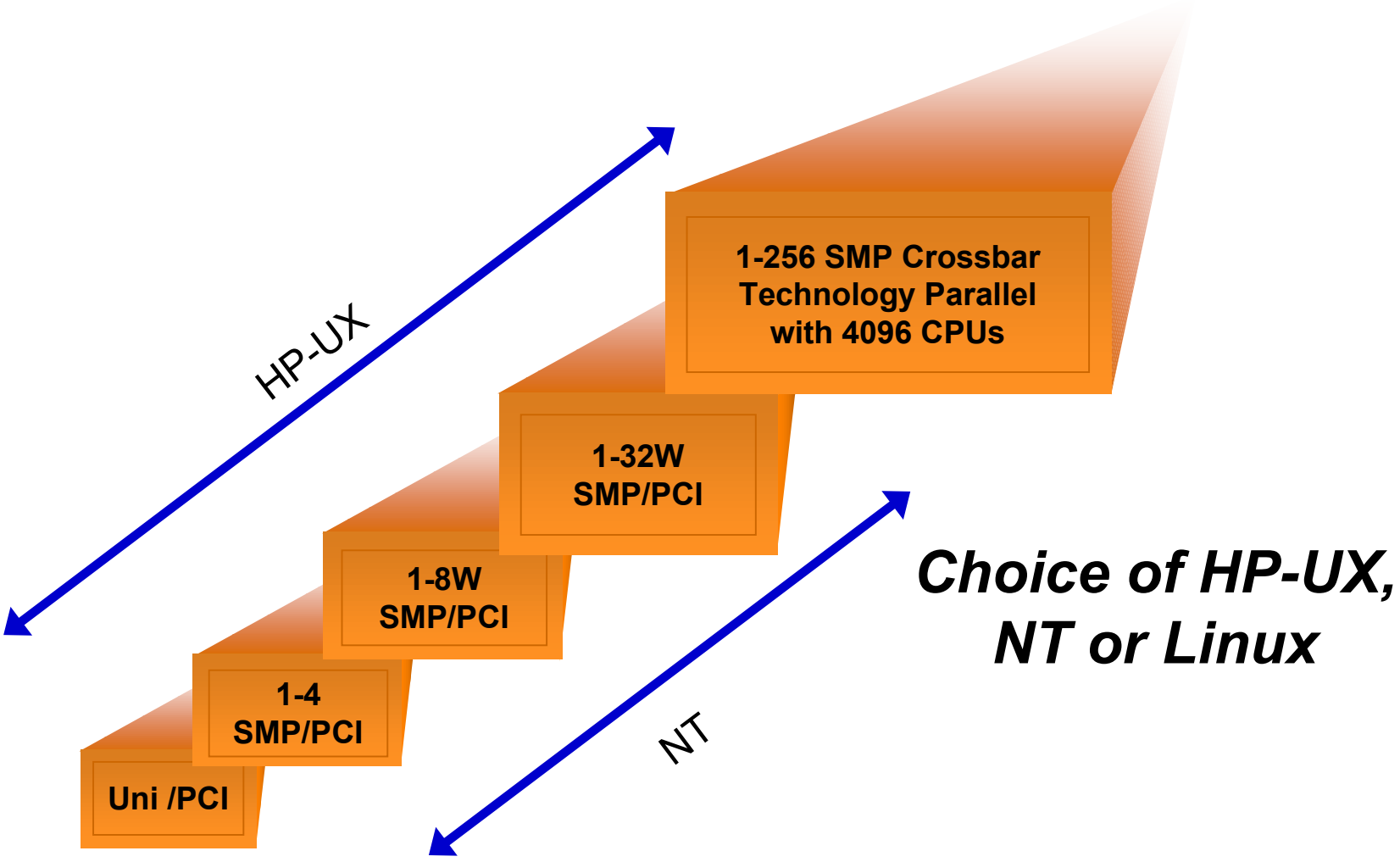


HP is a Leader in Both the UNIX and NT Markets



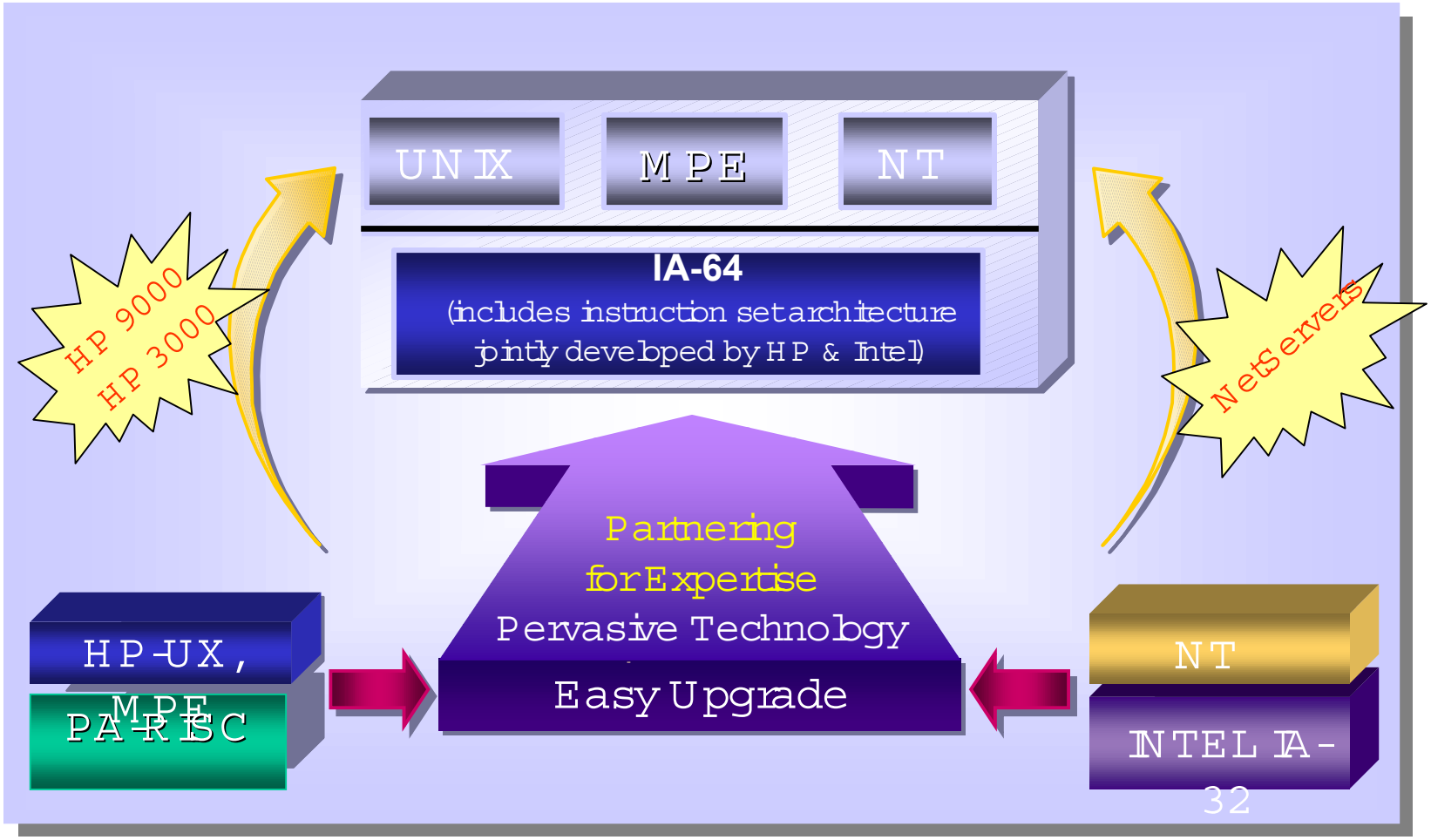
Today's HP Systems Platforms

HP's IA-64 System Platform Strategy: The Right Fit for Customer Environments

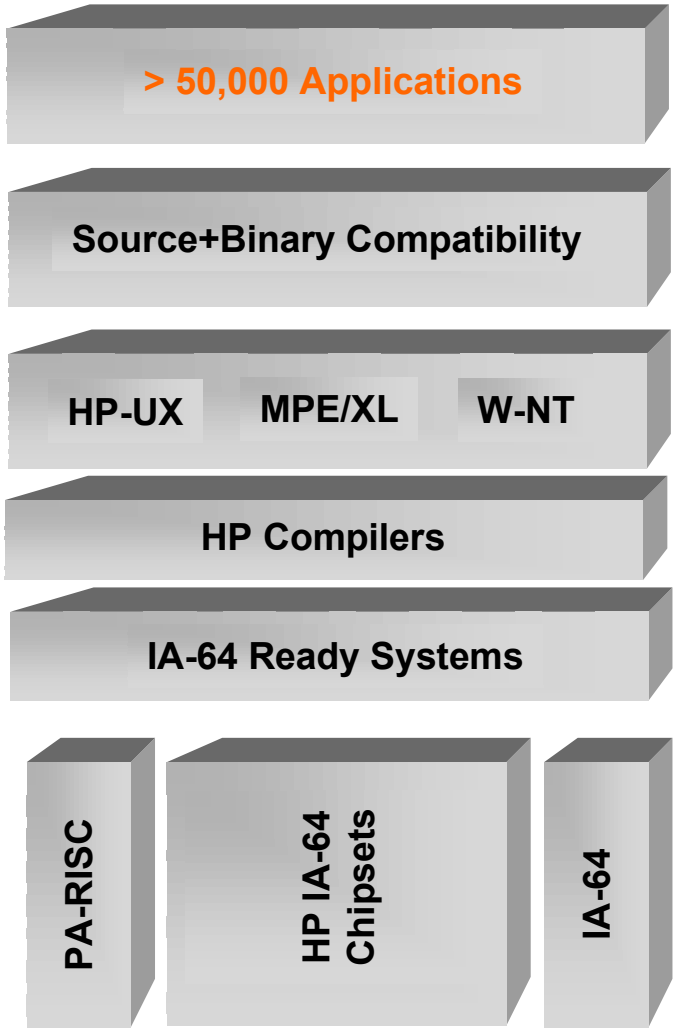


Choice of HP-UX, NT or Linux

IA-64: HP's Roadmap to the Future



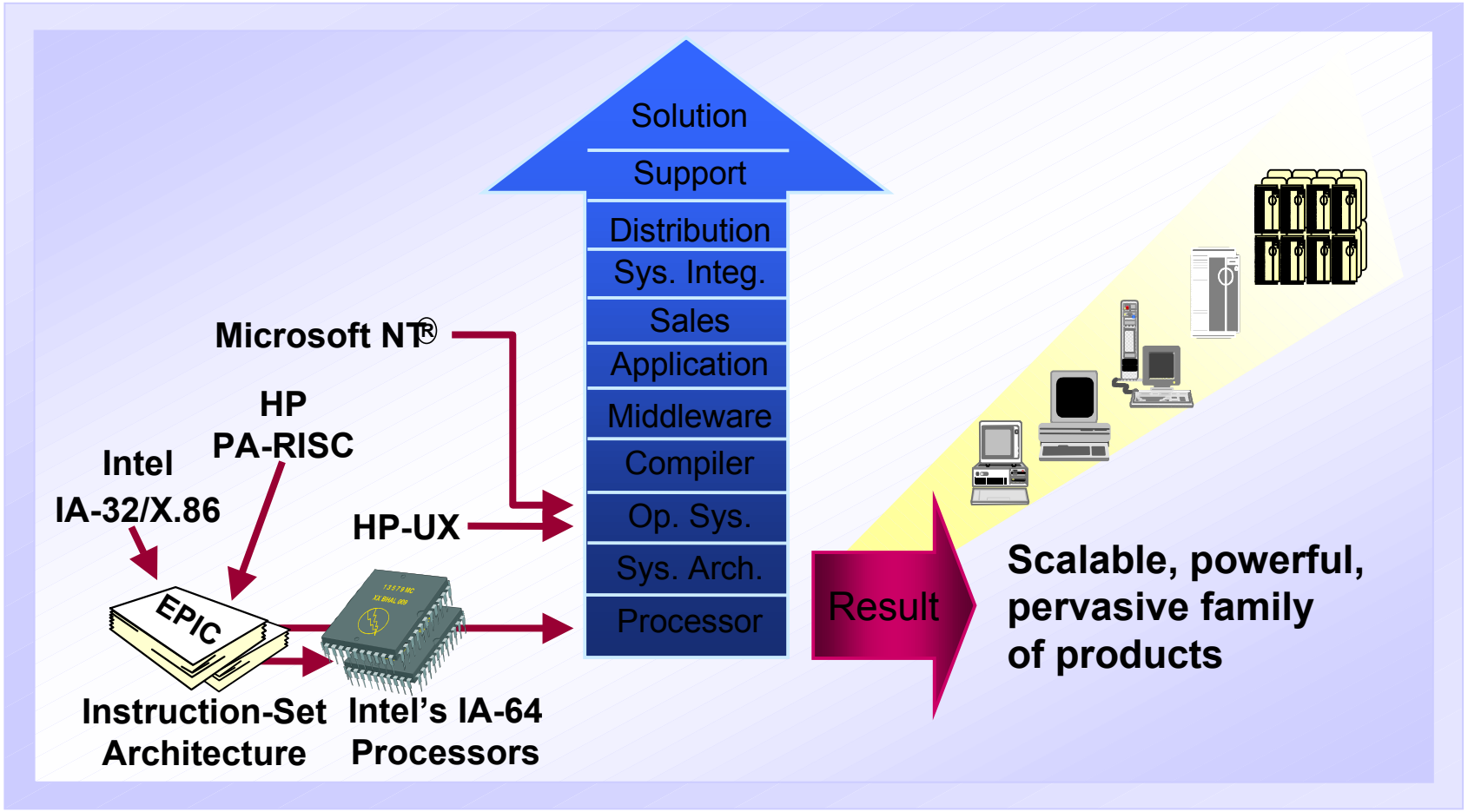
HP System Technology Environment



- **Investment Protection**
- **Seamless Transition**
- **Customers Chose When**
- **Systems Leadership**

- PA to IA-64 upgrades
- IA-64 Ready Systems
- Overlapping PA and IA-64 Processor Streams
- Binary Compatibility
- HP-UX II.x on both PA and IA-64 Systems

Differentiating in an Era of Merchant Technology

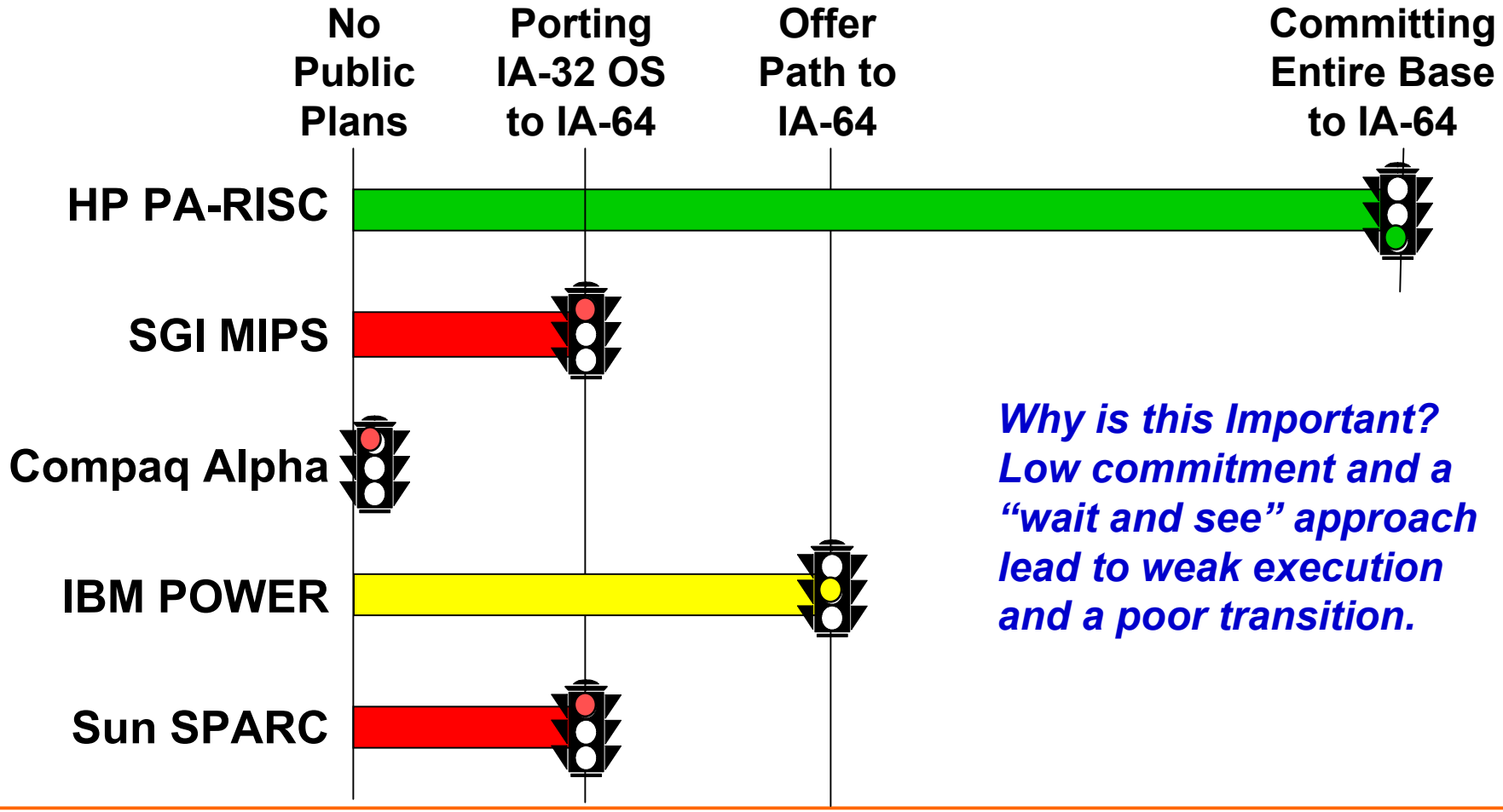


Architecting a Smooth Transition to IA-64

- **Hardware**
  - Parallel path of PA-RISC and IA-64
  - IA-64-ready board upgradable systems
- **Operating system**
  - HP-UX is IA-64 ready (minor update)
  - No administrator/operator interface changes
  - Collaboration with Microsoft on NT transition
- **Applications**
  - No forced application rewrites
  - No data migration
  - No forced applications recompiles

Which Vendors are Really Committed to IA-64

Some vendors' "IA-64 Commitments" are not as strong as others.



Why is this Important? Low commitment and a "wait and see" approach lead to weak execution and a poor transition.

IA-64 Transition Plans Compared

HP

Same box, same disks. Don't even copy the data.

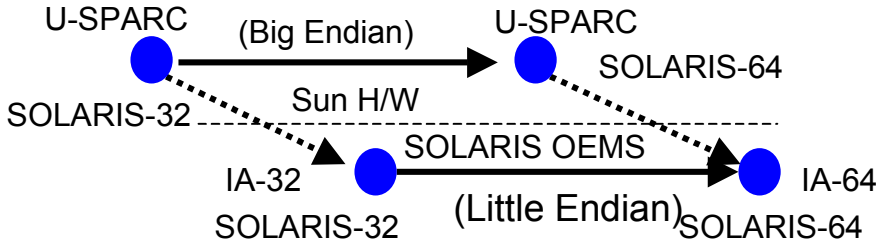
PA RISC to IA-64

HP-UX (same release), NT

- Binary Compatibility: Yes
- Data Compatibility: Yes
- Board Upgrade Yes

Sun

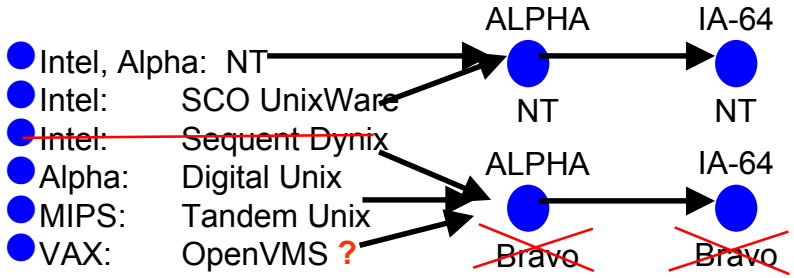
IA-32 story is OK--big problem is SPARC to Intel transition.



- Binary Compatibility Not from SPARC
- Data Compatibility Not from SPARC
- Board Upgrade Not from SPARC

Digital/Compaq

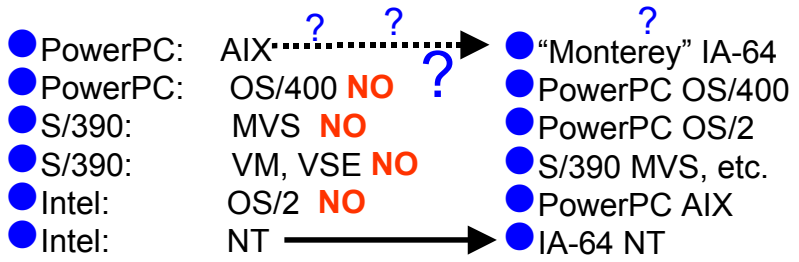
With Sequent dropping Bravo for Monterey, what now?



- Binary Compatibility: Not from Alpha
- Data Compatibility: Not from Alpha
- Board Upgrade: Not from Alpha

IBM

IBM's Monterey "Hail Mary pass" with SCO has many risks.



- Binary Compatibility Not from PowerPC
- Data Compatibility: Not from PowerPC
- Board Upgrade Not from PowerPC

HP-UX Operating Environment