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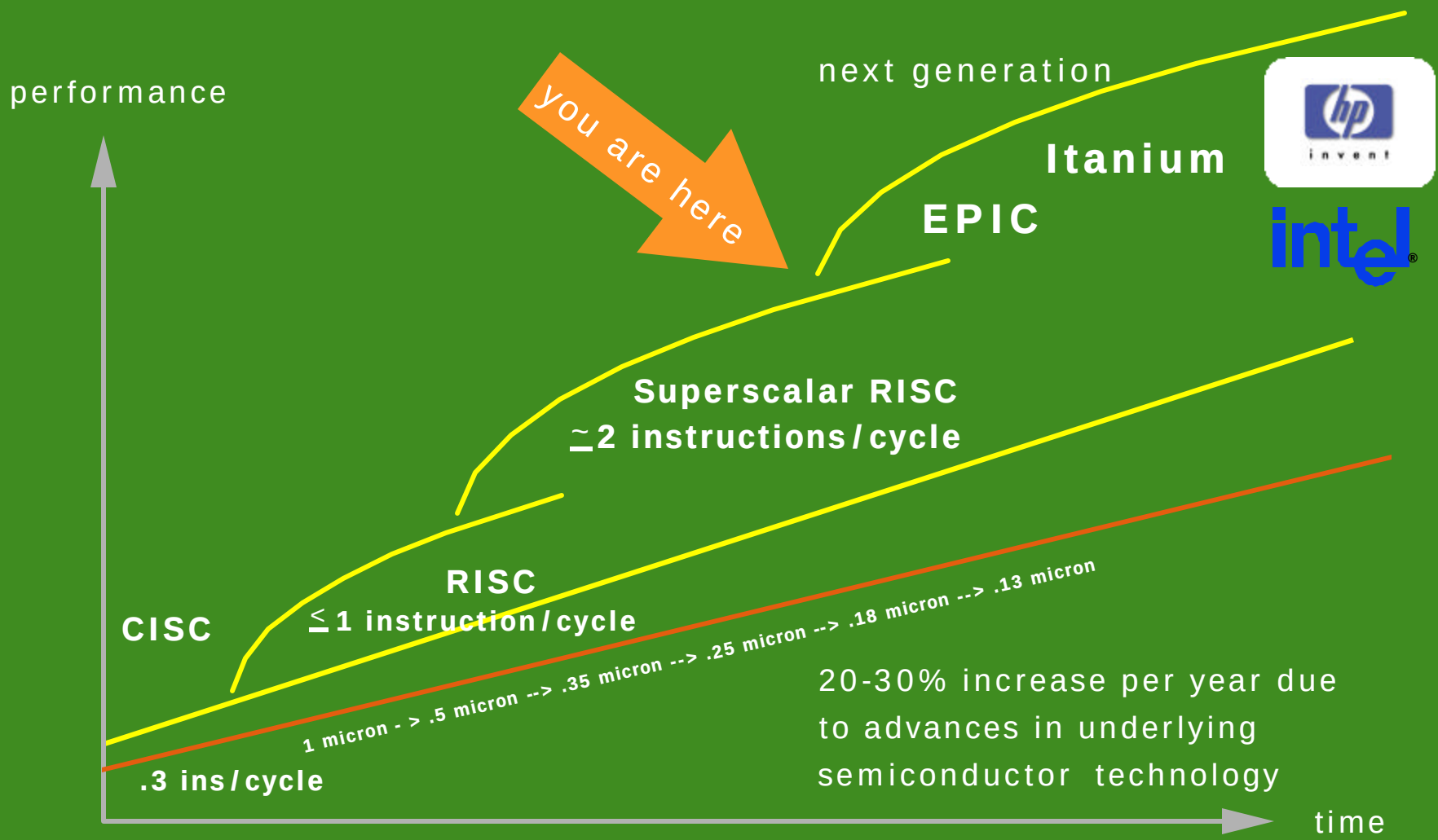
Processor Evolution



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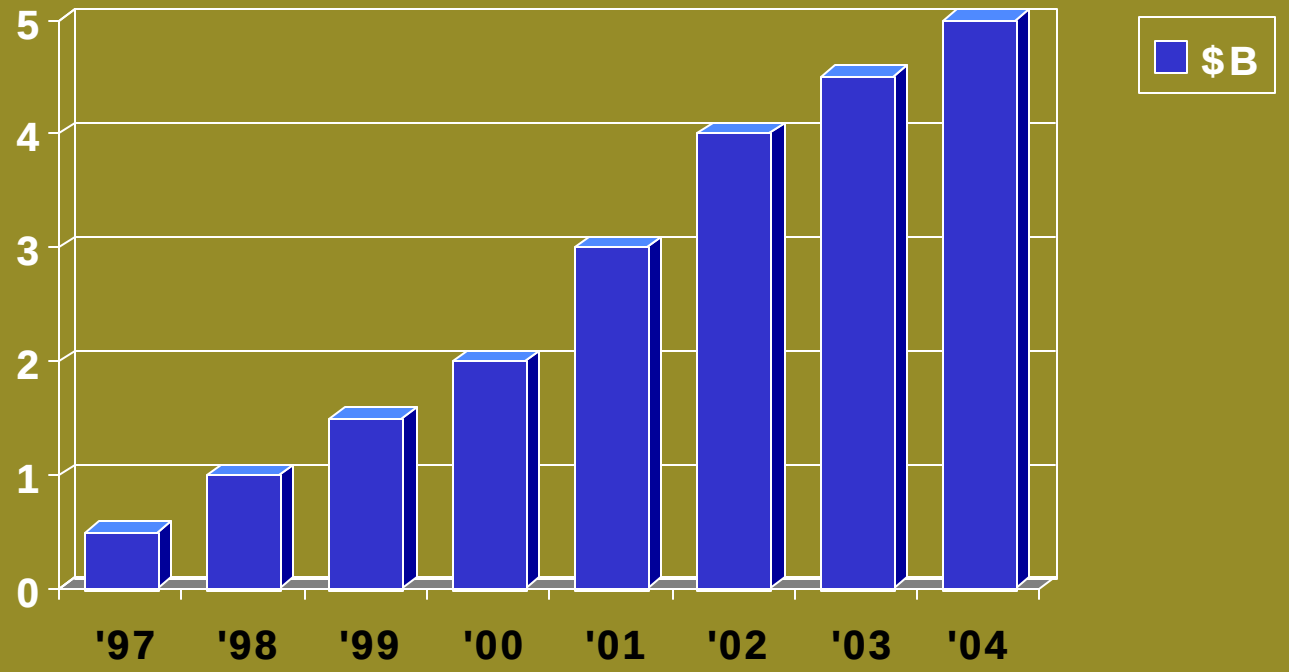
New Fab Costs Accelerating

How many proprietary RISC vendors can continue to invest?



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IPF: Built Upon the Hp/Intel History

- Leader in RISC and UNIX systems
- Advanced PA-RISC designs and compilers
- High-performance semiconductor processes

- Creator of world's most pervasive computing technology
- Excellent design tools
- Leadership in high volume semiconductor process

Breakthrough Performance
+ next generation beyond RISC
10's of thousands of applications
+ fully binary compatible with IA-32 and PA-RISC
+ supports applications for the world of e-services
Servers and Workstations
+ **hp**-ux, WIN64, and Linux support
Enterprise systems
+ desktops to supercomputers

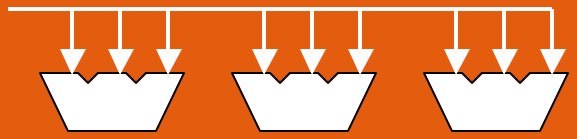
Today's Architectural Challenges

Resource constraints

- Too few registers
- Instruction scheduling

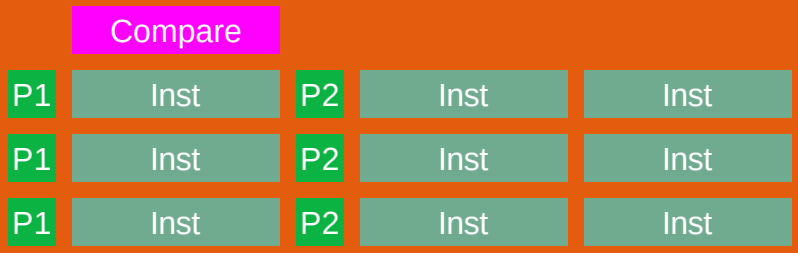
Floating-point Architecture

- **Parallel execution of multiple floating-point operations**
- **Higher (80-bit) precision arithmetic**
- **Large register set increases parallelism**



Predication and Speculation

- **Enhances instruction level parallelism**
- **Hides memory latency**

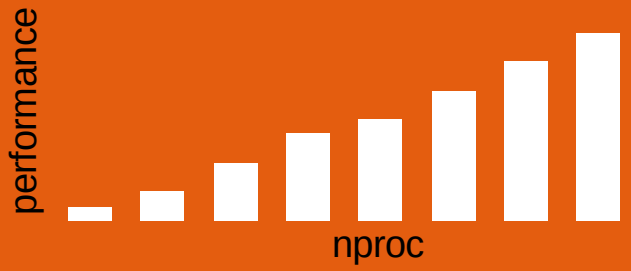


Instruction level Parallelism

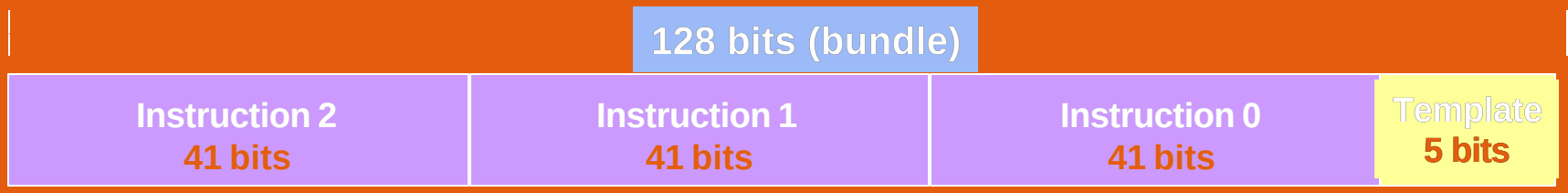
- **Increases processing efficiency**
- **Overcomes limitations of today's architectures**

Multiprocessor Scalability

- **Reduces time-to-solution**
- **Increases problem-solving capabilities**



IPF - An Explicitly Parallel Architecture



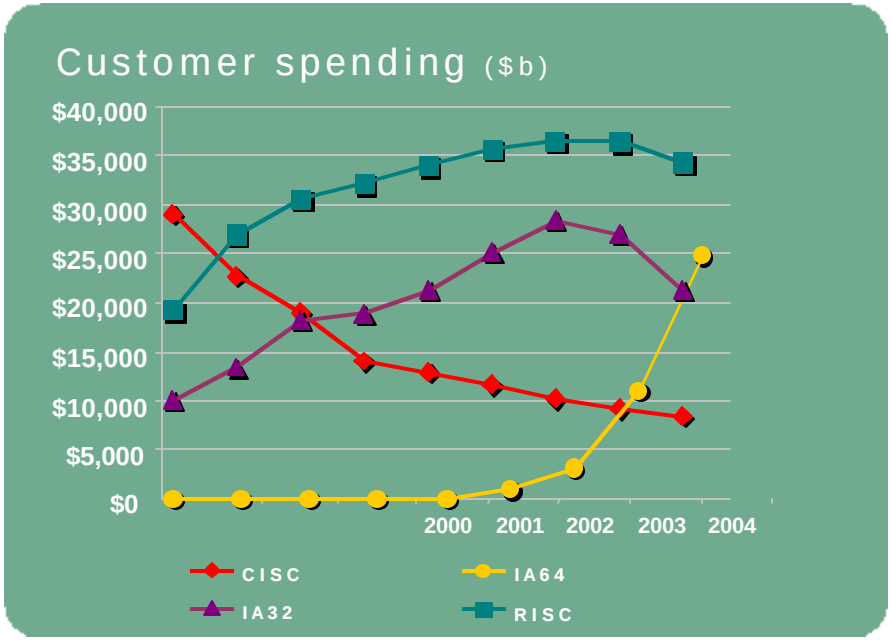
- IA-64 template specifies
  - The type of operation for each instruction
  - Intra-bundle relationship
  - Inter-bundle relationship
- Most common combinations covered by templates
  - Headroom for additional templates
- Simplifies hardware requirements
- Scales compatibly to future generations

HP offers
the
Smoothest Transition
to Itanium

Services and Support

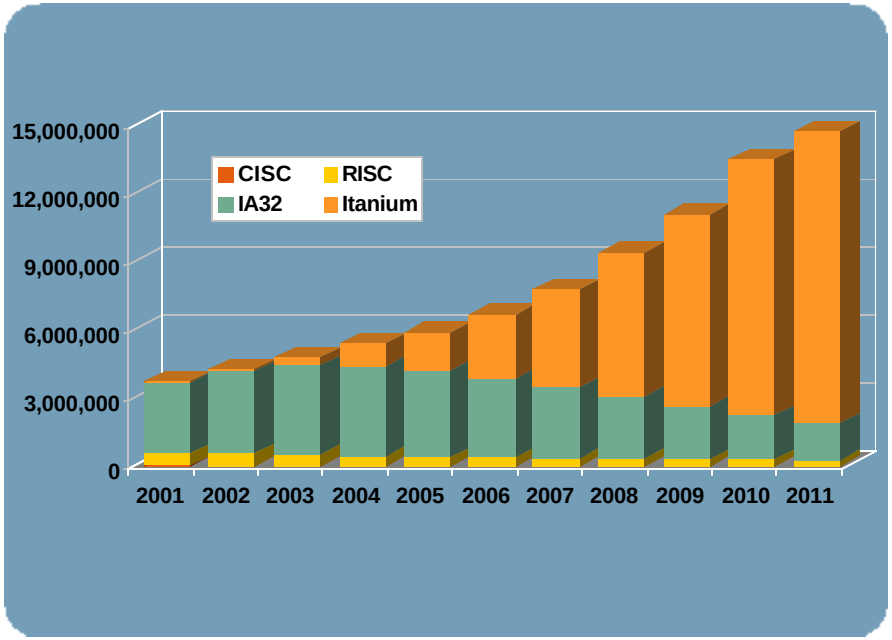
ISV and Developer programs
Implementation services

itanium® will be the pervasive computing platform for the future



Customer Benefits Include:

- Lower cost of computing
- Broader availability of applications
- More focus beyond the hardware
- More speed to meet business needs



Our Partners Are Committed to IPF

The software and services you need when you need them!

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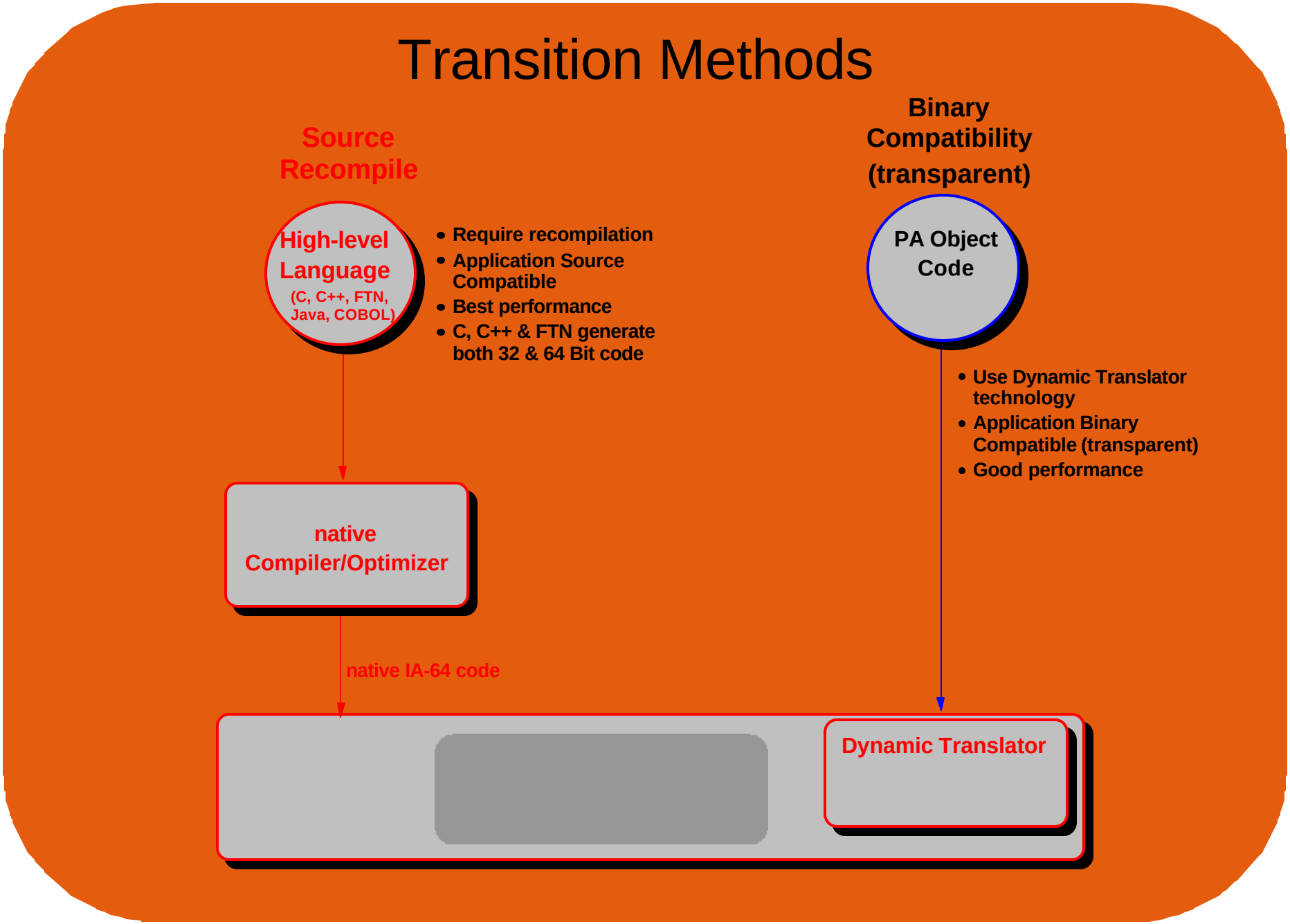
Industry Momentum Behind Itanium

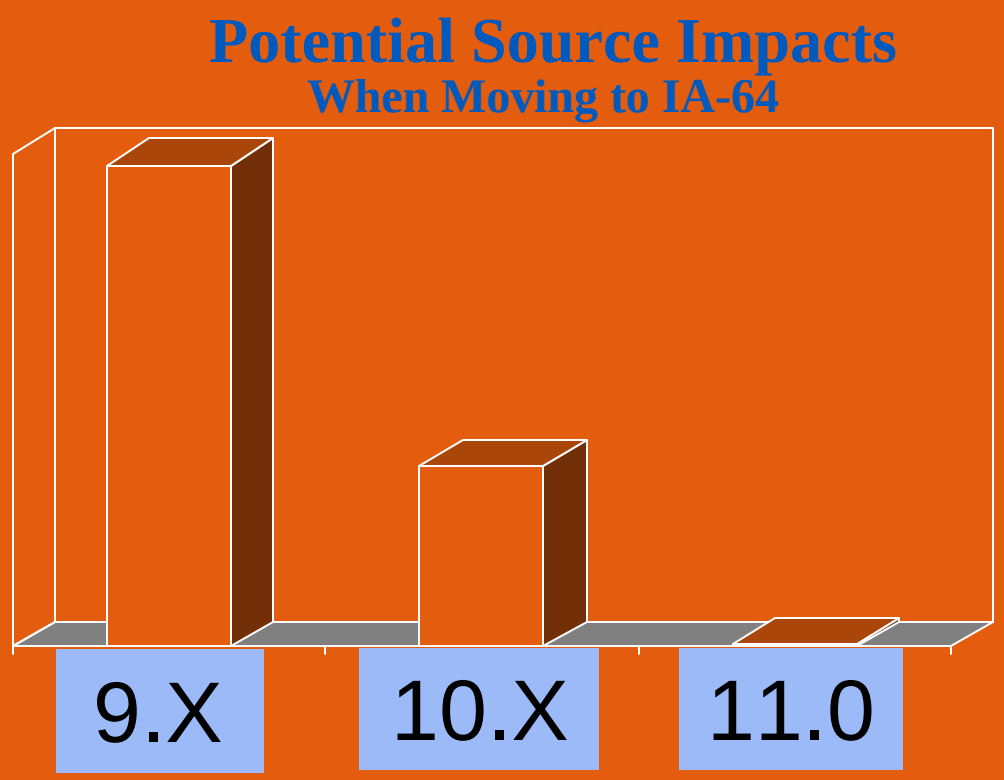
Every major platform has made a commitment to IPF

The Transition To Itanium

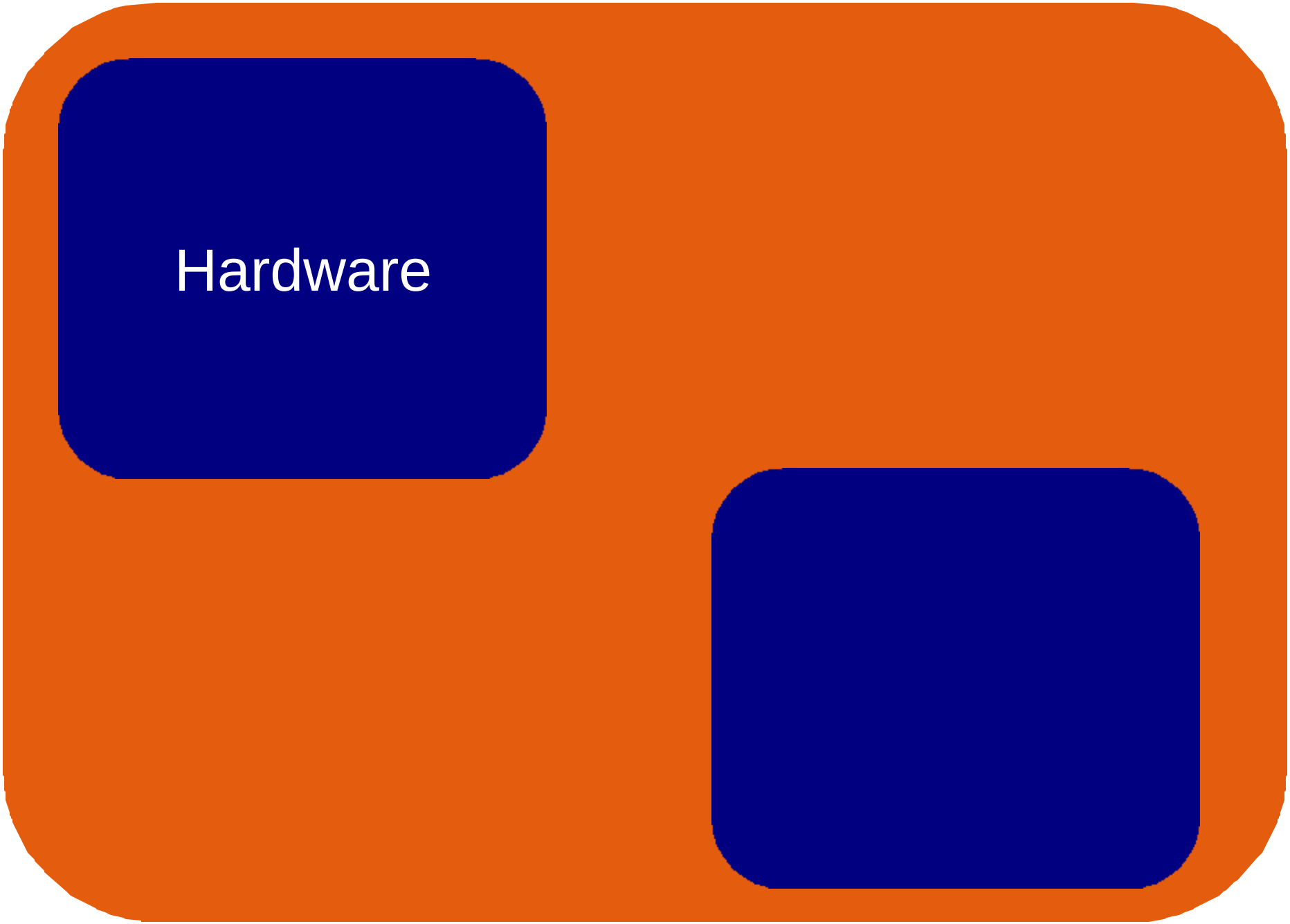
Transition Methods



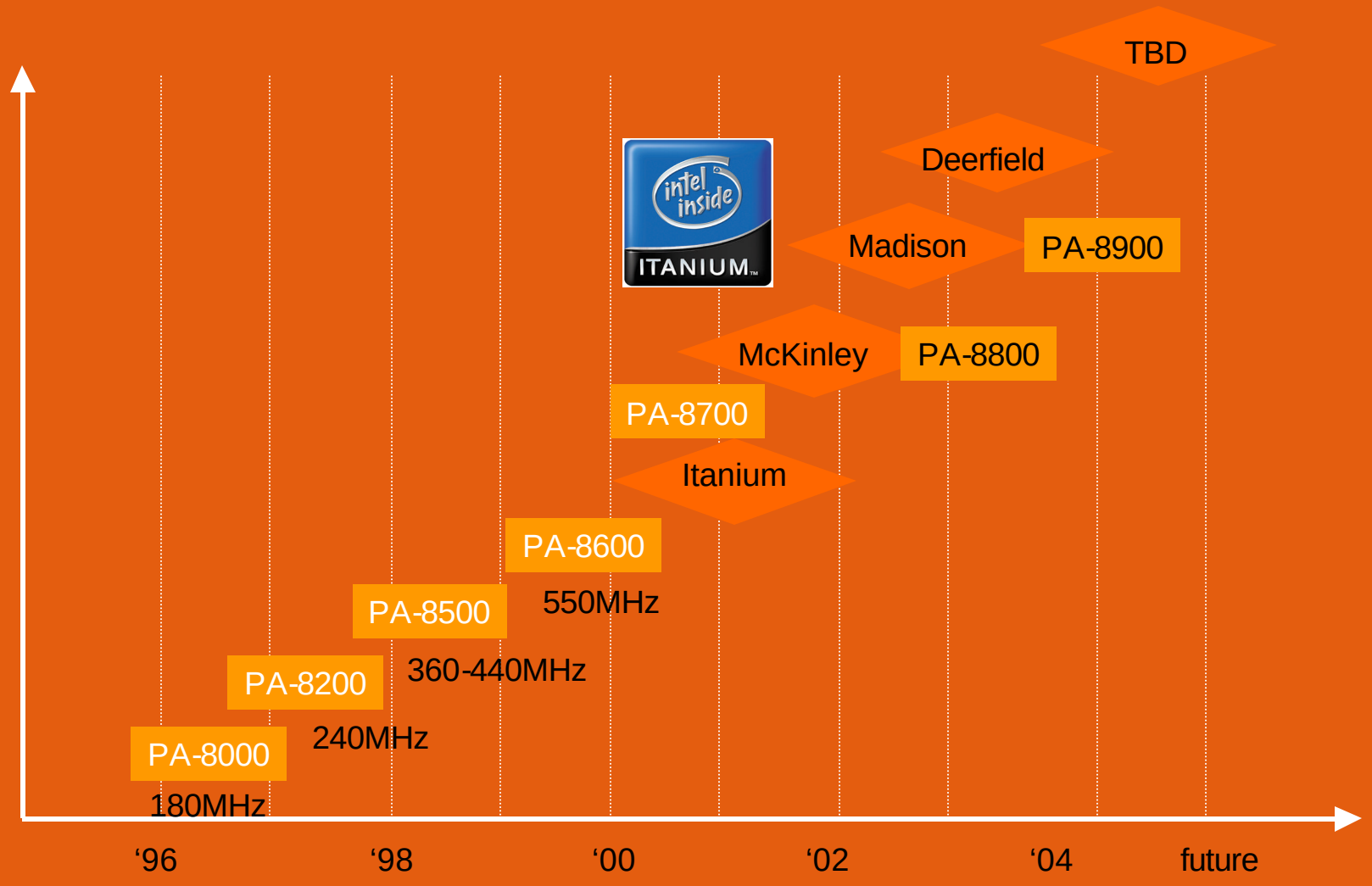
Source Code Impacts



A clear jumping-off point


Hardware

Itanium Co-existence With RISC



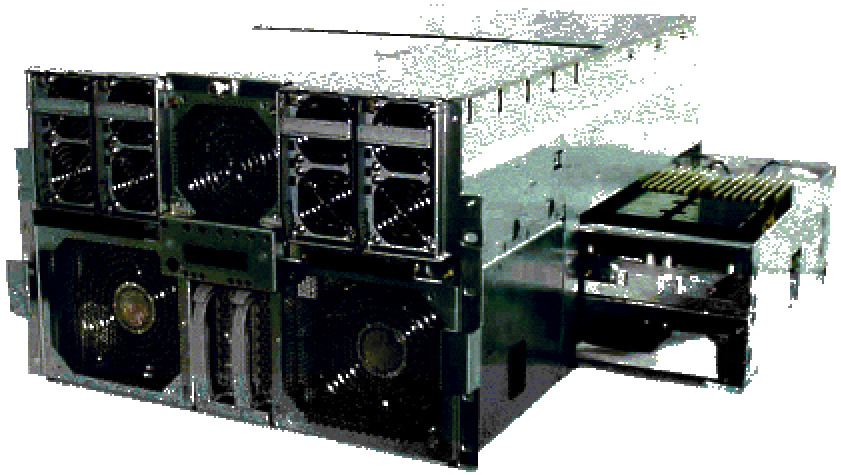
Big Sur…HP's First 2-way Itanium Workstation

- Dual 733 MHz Itanium processors
- 2MB high-speed cache
- 133 MHz front-side bus **(Intel 82460GX chipset)**
- 2GB SDRAM main memory
- **HP**'s multi-O/S strategy for Itanium: Windows, Linux, HP-UX support
- AGP-Pro high-performance graphics bus
- 3D-graphics adapter
- Mass storage: Ultra160 SCSI; DVD-ROM; LS-120

- 733 & 800mhz 2-4 way Itanium CPUs with 2M/4M L3 cache
- Up to 64 GB ECC SDRAM memory
- Two internal disks
- 10 PCI slots (8 are 66 MHz (4x) 3.3V hot plug, 2 are 33 MHz(2x), 5V non-hot plug)
- Hot-swap fans & power supply
- 7U rackmount chassis
- 48V distributed power, 4 (3+1) Autoranging power supplies (120 VAC 2x20amp or equiv)
- HP-UX 11i Ver 1.5

Introducing ‘Ironman’

Hp’s First 4-way Itanium Server!!



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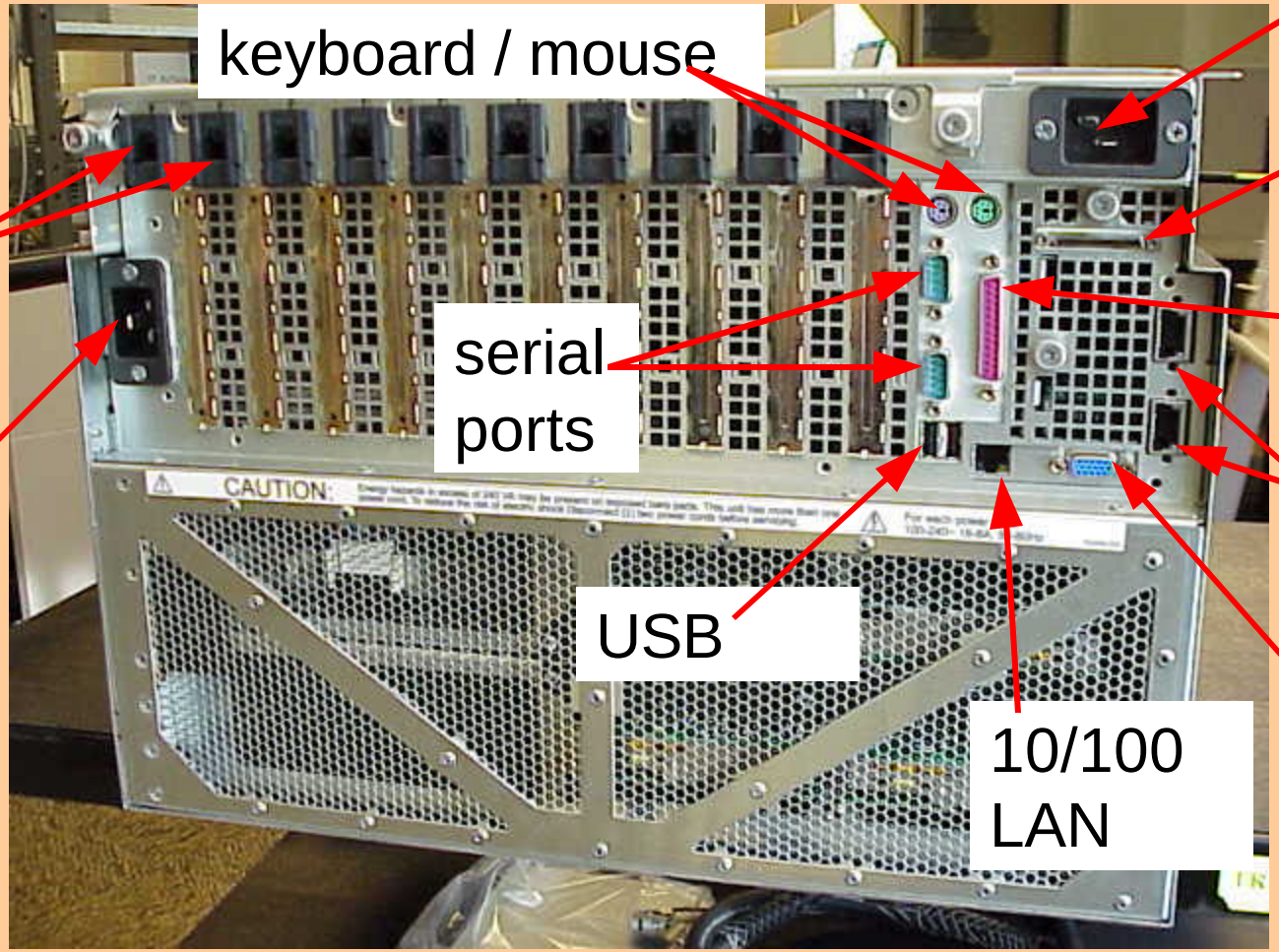
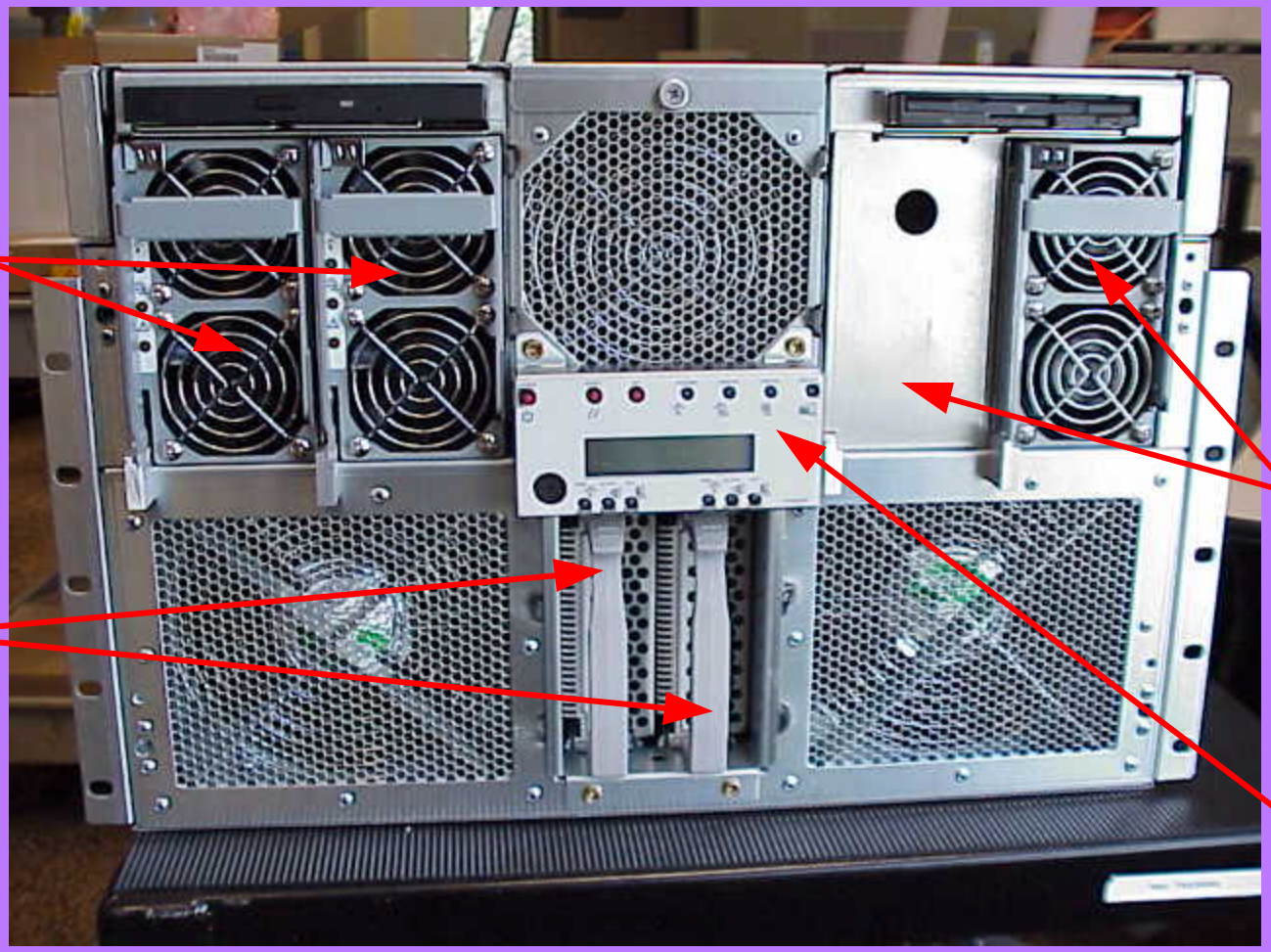
Ironman - rear view



Ironman - front view



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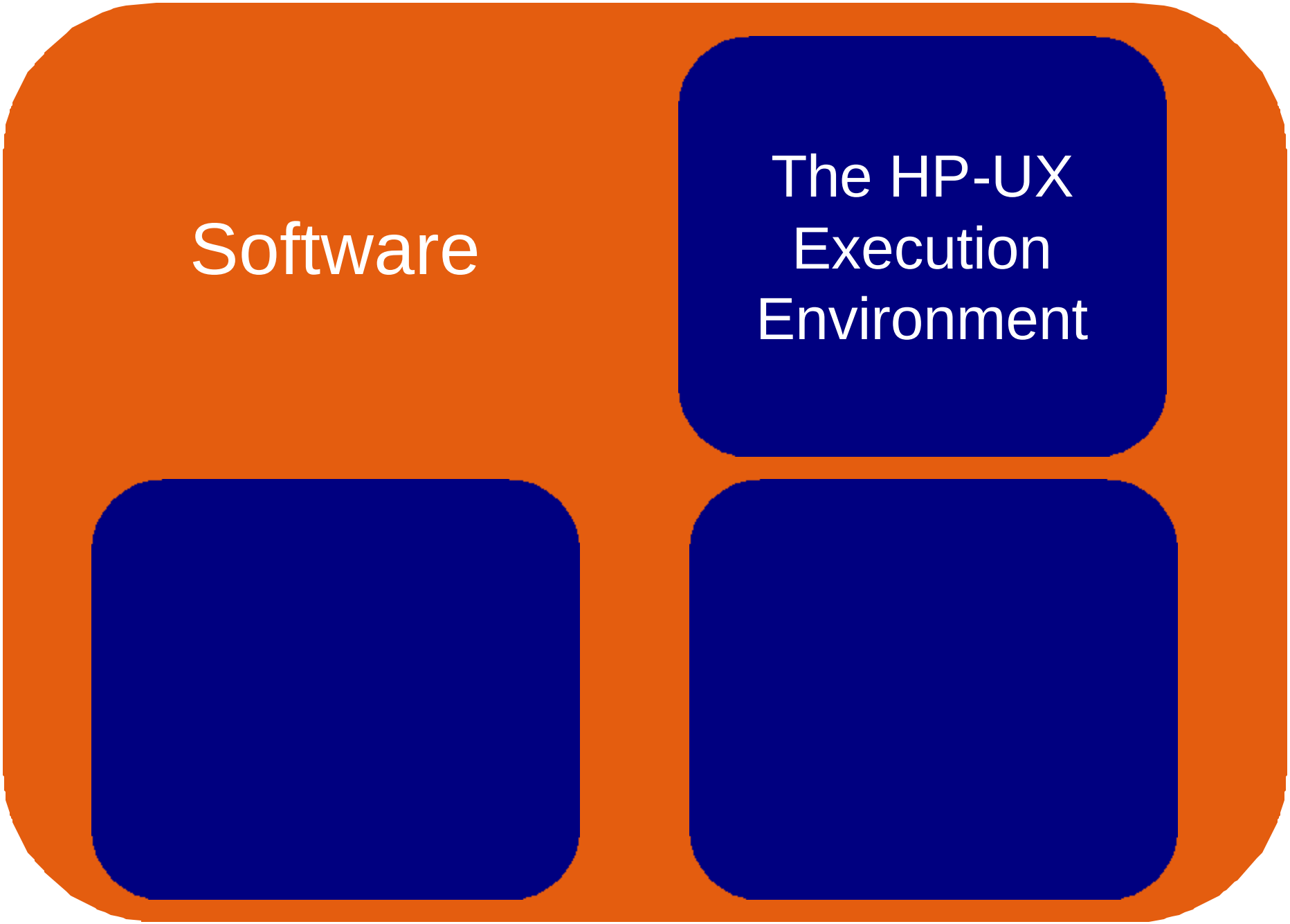

Software
The HP-UX Execution Environment

Binary Compatibility

Dynamic Translation

- **Supplied as part of HP-UX (4 libraries)**
  - **A boot loader and a translator for 32 and 64 bit in /usr/lib/hpux32/ (/usr/lib/hpux64)**
    - **Alternate path (32 bit) can be set in $ARIES32_PATH**
    - **Alternate path (64 bit) can be set in $ARIES64_PATH**
- **Has been tested with many programs: vi, xemacs, Netscape, Glance, GZIP, Apache, PERL and others.**
- **Quality: very solid.**
- **Continually being tuned for performance**

Limitations of Dynamic Translation

- Only pure 32-bit or 64 bit PA-RISC applications are supported. No mixed mode is allowed, whether PA/IA or PA32/PA64
- PA-RISC applications not supported on the PA-RISC version of a given release of HP-UX will not be supported on the IA-64 version of the release.
- Aries does not support applications compiled on HP-UX version 8.x or earlier.
- Aries does not support privileged PA-RISC instructions. Hence, device drivers and loadable kernel modules are not supported.

Limitations of Dynamic Translation (2)

- Aries does not support applications which use "/dev/kmem". These are applications that rely on kernel data structures, such as system administration programs. These will typically be available native on the IA-64 machine.
- Aries does not support timing-dependent applications. This includes applications that expect "real-time" response or assume that there is a consistency in the amount of time that it takes to execute a particular sequence of instructions.
- Aries will treat all floating-point NaNs (Not-a-Number) as quiet NaNs. Signalling NaNs are not supported.
- Aries does not support applications that use the ptrace(), ttrace() or profil() system calls. These are used by debuggers and profiling tools. Such tools are inherently not portable, and native debuggers are available.

Limitations of Dynamic Translation (3)

- Aries will not generate core dumps for applications that fail. While the application may fail with a core dump, the core will not be that of the PA application.
- Aries will not support applications that produce self-modifying code AND fail to properly synchronize their data and instruction caches. Self-modifying code is produced by applications like the JVM. Such applications must synchronize the caches to function correctly. HP-UX documentation specifies the correct way to do this.
- Aries will not support applications that read the status of the B-bit in the PSW (Process Status Word). PSW is a special purpose register used by PA-RISC chips. Most applications don't even know about this.

Limitations of Dynamic Translation (4)

- As Aries consumes a small amount of an application's virtual memory address space, it will not support applications that are nearly or completely maxed out on their virtual address space usage.
- Aries replaces vfork() with fork() as allowed under the HP-UX vfork() man page. Applications that rely upon the differences between fork() and vfork() are not supported.
- Aries will not support PA programs that load IA-64 shared libraries. In other words, mixing PA binaries with IA shared libraries is not supported. Aries is meant only for pure PA binaries, i.e., binaries that are either statically or dynamically linked with PA libraries only.

Aries: Failure Modes

- Bus error with or without core dump
  - If present, the core dump is an aries dump, not that of the application
- Missing library (will be common)
  - You may get a message, or you may not
- Aries limitation message – note that execution may not stop
  - Eg: Ptrace/ttrace
- Hang at some point, including at initiation

Dynamic Translation

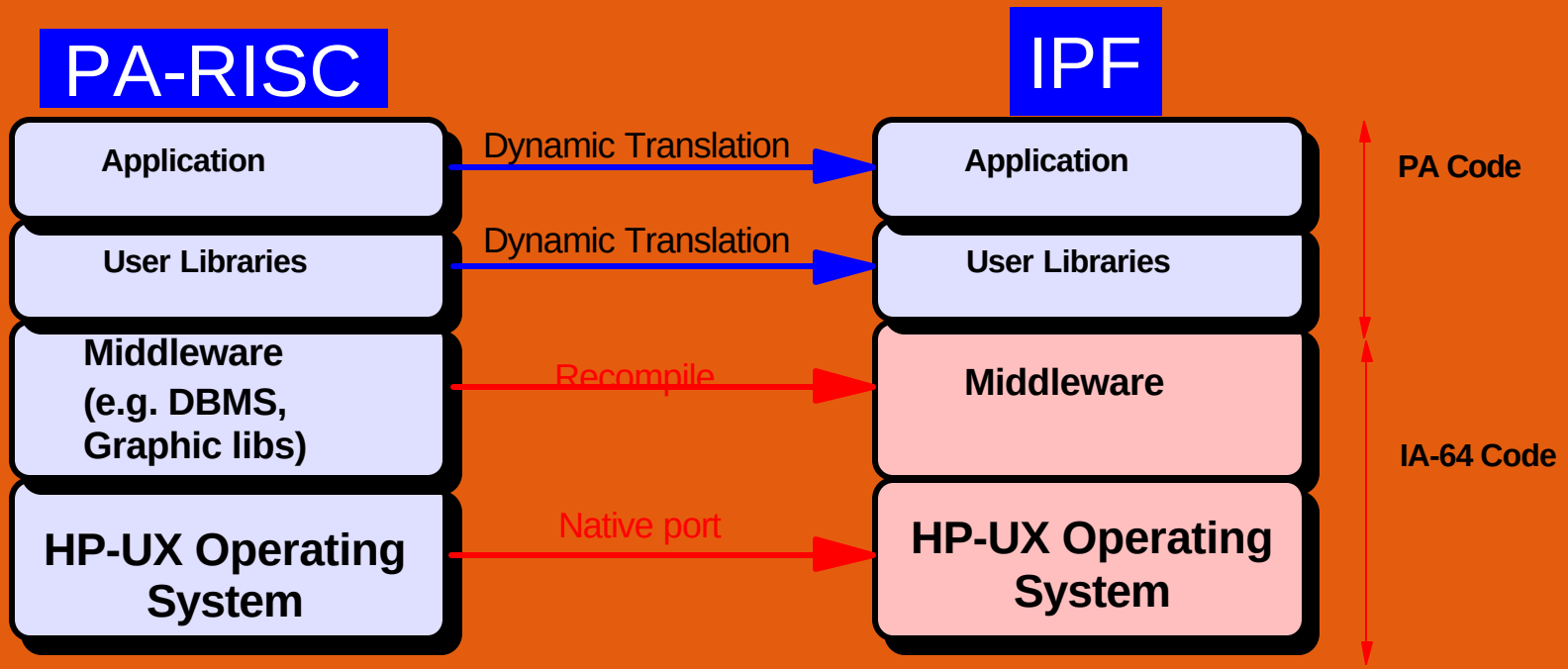
Specifying Options

- All options to aries are specified using a resource file: .ariesrc

- .ariesrc is searched for by aries as follows:
  - System wide (/usr/local/aries/.ariesrc), local to a user ($HOME/.ariesrc) or local to the current working directory (`pwd`/.ariesrc).

Execution Environment

- **A Mixed Environment**
- **Preserve the PA-RISC environment**
- **Allow incremental transition**



For More HP Itanium Info

- HP Itanium™ home page – this is a customer-facing site that carries architectural and market-related information of interest to potential customers, as well as the opportunity to sign up for a newsletter that carries features of interest to developers and customers. This is the site that will contain product info when the systems launch - http://www.ia64.hp.com
- HP Itanium™ future page – A subset of the home page, customers can get information on how Itanium™ will benefit the DCC market, the MCAE market, and the Chem/Pharm market, as well as some specific technical details - http://www.ia64.hp.com/future/index.html
- HP developers resource – contains most of the available technical documentation, white papers and developer kits for Itanium™ and Itanium™ Linux - http://www.devresource.hp.com/
- Intel Itanium processor family overview – our co-developers offer some specific technical market white papers and a section on the forthcoming workstations - http://www.intel.com/eBusiness/products/ia64/index.htm?iid=ebus+specfeature_IA64&
- Designing the future: HP Itanium partner program – mostly of interest to ISVs and developers, this site details the benefits and provides sign-up details for people who want to partner with us - http://www.hppartners.com/ia64/