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Author Name(s): Jon Davis
Company: Hewlett-Packard Company
Address: 19111 Pruneridge Avenue
Telephone Number: 408-447-4231
Fax Number: 408-447-4418
E-mail Address. jon_davis@hp.com

HP-UX 11i on Itanium: HP Is Ready, Are You?
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This is a paper about the creation of the next generation computing architecture and the rollout of this architecture with the HP-UX operating system. It explains the issues that the Itanium architecture seeks to address, the basic economics behind the Itanium architecture, and some of the details on the roll out of HP-UX 11i on the Itanium architecture.

The Collision of RISC Architectures with Moore's Law

The world of computing is about to witness an event of enormous consequences. That event is the industry transition to an industry-standard architecture that will span from the desktop to high-end computing and will bring PC-type pricing and price/performance with it. Just as the internet meant the end of proprietary networking protocols, so will this architecture spell the end of expensive, proprietary computing architectures. HP and Intel put this transition into play with the initial introduction of Itanium in mid-2001.

Although HP originally began as an instrumentation company, some of the background for this transition is in HP's recently established history as a successful innovator in computer architectures. In the late 1980's Hewlett-Packard launched an architecture that was to revolutionize the industry. That architecture was PA-RISC (Precision Architecture Reduced Instruction Set Computing), the first commercially available Reduced Instruction Set Computing (RISC) architecture in the industry. The previous generation of CISC (Complex Instruction Set Computing) architectures were based on the notion that the instructions had to be densely packed with functionality in order to maximize the amount of work done with each instruction. RISC architectures emphasized performance and price/performance over instruction functionality and found that both could be dramatically improved with a simplified instruction set which had far lower overhead compared to the CISC architectures. The validation of RISC architectures came in the succeeding years as both IBM and Sun Microsystems introduced RISC-based architectures in their major product lines (SPARC, RS/6000, PowerPC). RISC architectures have been a mainstay in the industry for the last 15 years.

In the mid-90's the RISC architectures began to collide with Moore's Law. Moore's Law, actually an observation of semiconductor density trends, stated that the component densities of microprocessors would double every 18 to 24 months. The effect of Moore's Law can be seen in the steady increase in the number of components contained in microprocessors as indicated in the following table.

Table 1 – Moore's Law as Illustrated by Increasing Component Density

Year	Processor	Number of transistors
1971	Intel 4004	2,250
1972	Intel 8008	2,500
1974	Intel 8080	5,000
1978	Intel 8086	29,000
1982	Intel 286	120,000
1985	Intel 386	275,000
1989	Intel 486 DX	1,180,000
1993	Pentium	3,100,000
1997	Pentium II	7,500,000
1999	Pentium III	24,000,000
2000	Pentium 4	42,000,000

This steady increase in the number of components that could be put into microprocessors began to have ramifications for computing architectures. With the steady increase in the number of components it became increasingly possible to process multiple instructions in parallel by creating multiple functional units. So, while previously a processor had a single arithmetic logic unit (ALU), processors now had multiple arithmetic logic units. With multiple functional units it was almost as if the processor had multiple processors within it. Processors with multiple functional units became known as super-scalar RISC processors.

However, simulation and deep instrumentation of RISC processors at HP Labs in the early 90's revealed a developing crisis for the RISC architectures. In computer programs, branches represent a decision between two sets of instructions. Current RISC architectures use a method called branch prediction to predict which set of instructions to load. When branches are mispredicted the whole path suffers a time delay. Through simulation and measurement it was determined that although today's processors use branch prediction techniques that are correct as often as 85 percent of the time, as much as 40 percent of an application's execution time may be due to the misprediction of branches.

This situation is being made worse by the increasing use of object-oriented languages such as C++ and Java. The enforced hierarchical nature of these languages has caused applications developed using them to contain many more branching possibilities than applications developed using the languages of previous generations.

It also turned out that as the number of functional units increased, the amount of logic required to find parallel processing opportunities increased by the square compared to the actual processing logic. So, with each doubling of component density, the amount of logic required to acquire parallel processing opportunities increased by a factor of 4. With this relationship between the functional units and the logic to discover parallel processing opportunities, it became obvious that RISC architectures would soon hit a

wall of diminishing performance improvements with new processors. HP Labs concluded that the looming performance crisis for RISC architectures presented a technical opportunity for the creation of a new architecture with the potential to dominate computing for the next 20 years. At the same time HP recognized that this could be an historic business opportunity. HP had watched the steady march towards the commodization of computing that had begun with desktop computing during the past 15 years and foresaw no reason why this could not continue into the high-end of computing. It was at this juncture that HP saw the opportunity to extend to enterprise computing the kind of price/performance that fueled the growth of desktop computing.

Designing for Compatibility

Investment protection has always been a hallmark of HP computing strategy. Since the later 1980's and early 1990's the commercial Unix computing business had grown into a multi-billion dollar business. It was a high priority to protect this business and the designers of the EPIC architecture looked for ways to ease the transition of HP-UX customers to the new architecture without impacting the performance potential of the new architecture. HP already had experience with one architectural transition; the transition of the HP 3000 16-bit architecture to the 32-bit PA-RISC architecture. This experience taught HP first-hand how perilous architectural transitions could be. Many of the lessons learned from that architectural transition were to be applied to the PA-RISC to Itanium architecture transition.

The Creation of the EPIC Architecture

HP Labs wrestled with the performance problem presented by the RISC architectures. The essential problem was how to easily introduce more parallelism for software whose exact execution path was maddenly difficult to predict. After investigating several alternative approaches, HP Labs developed the concept of explicitly parallel computing in which the compiler assumed the central role of creating multiple instruction streams that could be executed in parallel since it was uneconomical for the processor to perform this role. At the same time HP Labs developed the notion of predication or the process of determining the truth or falseness of a stream of instructions which represented one branching opportunity. This concept was a true breakthrough. Predication meant that it was cost-effective to process multiple branching opportunities in parallel and to discard the branches that failed or proved to be false. This approach to computing was given the name EPIC, an acronym that stands for Explicitly Parallel Instruction Computing.

The Itanium architecture is an implementation of EPIC. Itanium, the first processor of the Itanium Processor Family, has the ability to execute 4 code streams in parallel. Itanium2, the follow-on to Itanium, has the ability to execute 6 code streams in parallel. Future Itanium processors will have the ability to process additional code streams as processor densities increase.

Another problem that HP Labs wrestled with as part of the creation of EPIC was the issue presented by the relative speeds of memory and processor clocks. It is still true today that memory speeds are significantly slower than processor speeds. This has the effect that if a processor must wait for data to be retrieved from memory, several processor clock cycles will be lost. HP Labs developed the notion of speculation, that is, that the processor would not wait for data to be needed before requesting the data from memory. Hence, in the Itanium architecture the memory bus is kept busy all of the time retrieving data which may or may not be needed for processing. Doing so ensures to the maximum extent possible that the processor is never kept waiting for data to be retrieved from memory. The Itanium architecture also includes extensive functionality to ensure that data that becomes stale (is modified) is refreshed.

As noted earlier, some of the background for the design of the EPIC architecture was the need for compatibility with the PA-RISC architecture. HP knew well the dangers of architectural transition. A bumpy transition from 16 bits to 32 bits had helped cause the HP 3000 business to level off in the mid 1980's. The transition from PA-RISC to the Itanium processor family had to planned with the greatest care and attention to customer investment protection so that current customers would be retained. HP Labs, with this in mind, designed the EPIC architecture with the greatest possible compatibility with the PA-RISC architecture. The objective was to preserve as much as possible the software and expertise investment of HP-UX customers.

What Is Gained with the EPIC Architecture

The key advantages of the Itanium processor family are:

1) much higher performance potential thru predication and speculation

2) high-end performance at commodity pricing

The scalability of the Itanium architecture derives from the ability of the architecture to scale out and process multiple code streams simultaneously as integrated circuit manufacturing techniques improve. In this way the Itanium architecture does not suffer from the inherent lack of scalability that the RISC architectures are encountering. The original Itanium processor could process 4 code streams simultaneously. Itanium 2 can process 6 code streams simultaneously. Future Itanium processors will expand the number of code streams that can be processed simultaneously.

The pricing advantages of the Itanium processor family derive from being manufactured on the same manufacturing lines as IA-32 which allow the Itanium processor family to enjoy the same manufacturing economies of scale as commodity PC processors.

Preserving the Intellectual Property of HP-UX Customers

As noted earlier, it was a top priority of the HP-UX Itanium program to preserve the intellectual property of HP-UX customers, that is, the investments in software and also the expertise in tuning and operating HP-UX systems.

For this reason, HP-UX 11i version 1.5, the first version of HP-UX 11i for the Itanium processor family, was built from the same source code as HP-UX 11i on PA-RISC. This means that:

1) HP-UX 11i for Itanium has the same "look and feel" as HP-UX 11i on PA-RISC:
    a. HP-UX 11i has the same user interface on both architectures
    b. The layered software products (Process Resource Manager, System Inventory Manager, Intrusion Detection, MC/Serviceguard, etc.) are the same on both architectures.

2) HP-UX 11i for Itanium benefits from the 64-bit maturity of HP-UX 11i (HP-UX 11i on PA-RISC has experienced the lowest defect submission rates of any HP-UX release to date)

In addition to a common "look and feel" and common layered software products, HP-UX 11i on Itanium features other key compatibilities with HP-UX 11i on PA-RISC:

1) HP-UX 11i features application source code compatibility across the PA-RISC and Itanium architectures. This means that application programs from HP-UX 11i on PA-RISC can be made into native Itanium applications with recompilation; no source code modifications are necessary regardless of whether the application is 32 or 64 bits on PA-RISC (HP-UX 11i on the Itanium Processor Family supports both 32-bit and 64-bit applications even though Itanium is a 64-bit architecture). However, converting a 32-bit PA-RISC application into a 64-bit Itanium application may require some source code changes.

2) HP-UX 11i on the Itanium processor family has the same data formats as HP-UX 11i on PA-RISC. This means that there is complete data interoperability between the two architectures. This interoperability allows the seamless integration of HP-UX 11i Itanium systems into a network of HP-UX 11i PA-RISC systems.

3) HP-UX 11i on the Itanium processor family can transparently execute PA-RISC binaries. This is possible through the Aries dynamic code translation technology which is a built-in, integrated part of every copy of HP-UX 11i on the Itanium Processor Family. Performance in code translation mode is likely to be less than native mode but dynamic code translation ensures that all PA-RISC applications can execute on the Itanium architecture without recompilation.

4) HP-UX 11i on the Itanium processor family features networking that is compatible with the networking of HP-UX 11i on PA-RISC, thus providing interoperability between HP-UX 11i PA-RISC systems and HP-UX 11i Itanium systems.

Binary compatibility proved to be challenging. Typically, binary incompatibility is the hurdle that causes most migrations to fail or be extremely painful. The EPIC design team realized this and thought long and hard about how the transition from PA-RISC could be eased. Clearly, it was impossible to provide complete compatibility at the instruction level. Asking the EPIC architecture to provide binary compatibility with the PA-RISC architecture would likely cause unacceptable performance for both. The answer was the Aires dynamic code translation technology which is a standard integrated component with every copy of HP-UX 11i on Itanium. Whenever a PA-RISC binary is launched on an Itanium system the Aries dynamic code translation technology is automatically and transparently invoked to dynamically translate the PA-RISC binary into Itanium instructions.

The Partnership with Intel and Moore's Second Law

While HP Labs wrestled with the creation of a next generation architecture that would overcome the performance bottlenecks that RISC architectures were encountering, HP management was wrestling with the funding that the rollout of a new processor would require. In addition to his first law, Gordon Moore had also postulated a second law which stated that the fabrication facilities double in cost with every new generation of microprocessors. It was estimated that going into production for the new architecture could cost the prohibitive amount of 5 to 6 billion dollars. It was at this point that HP took a direction it had never pursued previously. On the basis of the economics involved, it was decided that HP would seek to partner with Intel, the world's premier semiconductor manufacturer, to bring the new architecture to market. In 1994 HP, with a track record of successful innovation in computer architecture by bringing the first RISC architecture to market, formed a partnership with Intel to bring the EPIC architecture to market. Intel received access to the EPIC architecture in return for designing and manufacturing processors based on the EPIC architecture. As the designer and manufacturer for processors based on the EPIC architecture Intel had the opportunity to access the high end and data center, something it had never enjoyed previously.

The partnership between HP and Intel on the EPIC architecture that began in 1994 brought together HP's expertise in architecture and Intel's expertise in mass production of processors. This partnership has created a dynamic that will forever change the face of the information industry.

Charting the Transition

With a design and manufacturing partner determined, HP turned its attention to planning the transition for HP-UX 11i. As it turned out, the transition of HP-UX 11i to the Itanium processor family would require several releases of HP-UX 11i. The following table shows the major releases, their timeframe, and content.

Table 2 – HP-UX 11i Releases for the Itanium Processor Family

HP-UX Release	Timeframe	Release Identifier	Packaging	Content
HP-UX 11i version 1.5	Mid-2001	B.11.20	Operating System Media, Application Release	HP-UX 11i, selected independent software units
HP-UX 11i version 1.6	Mid-2002	B.11.22	HP-UX 11i Operating Environment, HP-UX 11i Technical Computing Environment for Servers, Application Software	Enterprise-quality HP-UX 11i, nearly all independent software units
HP-UX 11i version 2	Mid-2003	B.11.23	HP-UX 11i Internet, Enterprise, Mission-Critical, and Technical Computing Operating Environments, Application Release	Enterprise-quality HP-UX 11i, equivalent functionality except for vPars (Virtual Partitions), large scale adoption by ISVs

Content of the HP-UX 11i version 1.5 Release

HP-UX 11i version 1.5 was the very first release of HP-UX 11i on the Itanium processor family. Version 1.5 supported the very first HP Itanium servers, the rx4610 and the rx9610. As the first release, version 1.5 did not have broad support from HP's independent software units (MC/Serviceguard, Process Resource Manager, etc.). Table 3 below shows the content of HP-UX 11i version 1.5.

Table 3 – HP-UX 11i version 1.5 Release Content

Product Number	Product Name	Description	Mode
B9415AA	Apache	Apache Web Server	PA
B3899BA* B3901BA	C/ANSI C Dev	HP C/ANSI C Developer Bundle	IPF
B3907DB* B3909DB	Fortran	Fortran compiler	IPF
GigEther-00	Gigabit Ethernet	PCI Gigabit Ethernet LAN driver	IPF
B3691AA* B3693AA B3691AJ* B3693AJ	Glance Plus Glance Plus - Jpn	GlancePlus HP9000 Server Japanese GlancePlus HP9000 Server	IPF/PA
B6060BA	MPI	HP Message Passing Interface	IPF
B5118CA* B3929CA	Online JFS	Online Backup for JFS	IPF
B9116AA	VxVM – Full	Veritas Volume Manager – Full	IPF
B3911DB* B3913DB	ANSI C++	HP ANSI C++ compiler	IPF
B3394BA	Dev Kit	HP-UX Developer's Toolkit. Tools for user interface development	IPF/PA
B6061AA	MLIB	HP Parallel Math Library	IPF
B4580AA	STK	HP-UX 11i Version 1.5 Software Transition Kit	IPF
B9789AA B9788AA	Java 2 RTE 1.3 Java 2 SDK 1.3	Java 2 RTE/SDK 1.3 Run Time Environment and Software Development Kit (Beta version) Product Release version available (Summer 2001)	IPF
B4965AA* B4967AA B4965AJ* B4967AJ	MWA Svr MWA Svr - Jpn	Measureware Server –Tool for viewing system data Japanese Measureware Server	IPF/PA
B5403BA* B2491BA	MirrorDisk/UX	Disk Mirroring for HP-UX	IPF
B8342AA	Netscape	Netscape Communicator	PA
B2432EB* B2435EB	Object Cobol RTS	HP Micro Focus Object Cobol Runtime System	PA
B6960AA	OmniBack	OmniBack Backup Software	PA
B6836AA	OpenGL	Open Graphics Language	IPF
FibrChanl-00	Fibre Channel	PCI Fibre Channel LAN Driver	IPF

Content of the HP-UX 11i version 1.6 Release

HP-UX 11i version 1.6 achieved shipment release in August of 2002. HP-UX 11i version 1.6 is packaged as an HP-UX 11i Operating Environment (Enterprise and Mission-Critical Operating Environments are not available until version 2) with all of the attendant benefits: single install, single product number, single support contract. Table 4 shows the content of the version 1.6 release. HP-UX 11i version 1.6 provides binary compatibility with HP-UX 11i version 1.5.

HP-UX 11i version 1.6 features broad participation of HP independent software units with only a few to be added with version 2. Table 4 below shows the content of HP-UX 11i version 1.6.

Table 4 – HP-UX 11i version 1.6 Release Content

Product Number	Product Name	Description	Part of HP-UX 11i Version 1.6 Operating Environment	Mode
B3899BA	CDev	ANSI C Developer's Kit for Workstations	No	Itanium Processor Family
B3901BA	CDev	ANSI C Developer's Kit for Servers	No	Itanium Processor Family
B8724AA	CIFS	Common Internet File System Client	Yes	Itanium Processor Family
B8725AA	CIFS	Common Internet File System Server	Yes	Itanium Processor Family
B2432EB	COBOL	Object-Oriented Cobol Runtime	No	PA
B2435EB	COBOL	Object-Oriented Cobol Runtime	No	PA
B3911DB	CPlusPlus	ANSI C++ for Workstations	No	Itanium Processor Family
B3913DB	CPlusPlus	ANSI C++ for Servers	No	Itanium Processor Family
B3394BA	DevKit	HP-UX Developers Kit	No	Itanium Processor Family
B5736DA	EMS HA	High Availability Monitors	No	Itanium Processor Family/PA
B7609BA	EMS Framework	Event Management System Framework	Yes	Itanium Processor Family/PA
A5158A	FibreChannel	1-port PCI 2x Fibre Channel Adapter	No	Itanium Processor Family
A6795A	FibreChannel	XL2 PCI Adapter	No	Itanium Processor Family
B3907DB	Fortran	FORTRAN 90 for workstations	No	Itanium Processor Family
B3909DB	Fortran	FORTRAN 90 for servers	No	Itanium Processor Family
A4926A	GigabitEthernet	PCI Gigabit 1000Base-SX Adapter	No	Itanium Processor Family
A4929A	GigabitEthernet	PCI Gigabit 1000Base-TX Adapter	No	Itanium Processor Family
A6794A	GigabitEthernet	GbE PCI-X 1000Base-T	No	Itanium Processor Family
A6825A	GigabitEthernet	GbE PCI-X 1000Base-T	No	Itanium Processor Family
A6847A	GigabitEthernet	GbE PCI-X 1000Base-SX	No	Itanium Processor Family
B3691AA	Glance	OpenView GlancePlus M/M for Workstations	No	PA
B3691AA TRY	Glance	OpenView GlancePlus M/M Trial Copy for Workstations	No	PA
B3693AA	Glance	OpenView GlancePlus M/M for Servers	No	PA
B3693AA TRY	Glance	OpenView GlancePlus M/M Trial Copy for Servers	No	PA
B6836AA	GraphicsDevKit	OpenGL	No	Itanium Processor Family/PA
B8342AA	GraphicsDevKit	Netscape Communicator Browser (4.79)	No	PA
B9415AA	HP Apache	HP Apache-based Web Server	Yes	Itanium Processor Family
J5083AA	IDS-UX	HP Intrusion Detection System	Yes	PA
B5725AA	Ignite/UX	HP-UX Installation Utilities	Yes	PA
B9788AA	Java	HP-UX SDK,LTU, Java(tm) 2 Platform 1.3	No	Itanium Processor Family/PA
B9789AA	Java	Java 2 Platform 1.3 Runtime Environment LTU for HP-UX	Yes	Itanium Processor Family/PA
J5849AA	Kerberos	Pam Kerberos	Yes	Itanium Processor Family/PA
B4965AA	MeasureWareAgent	OpenView Performance Agent for Workstations	No	Itanium Processor Family/PA
B4965AA TRY	MeasureWareAgent	OpenView Performance Agent Trial Copy for Workstations	No	Itanium Processor Family/PA
B4967AA	MeasureWareAgent	OpenView Performance Agent for Servers	No	Itanium Processor Family/PA
B4967AA TRY	MeasureWareAgent	OpenView Performance Agent	No	Itanium Processor Family/PA
B2491BA	MirrorDisk	MirrorDisk/UX for Servers	No	PA
B5403BA	MirrorDisk	MirrorDisk/UX for Workstations	No	Itanium Processor Family/PA
B6061AA	MLIB	Mathematical Libraries	Yes	Itanium Processor Family
B6060BA	MPI	Message Passing Interface	Yes	Itanium Processor Family
B6960BA	Omniback	OpenView Omniback II	No	PA
B3929CA	Online	Online JFS 800 (version 3.3)	No	Itanium Processor Family/PA
B5118CA	Online	Online JFS 700	No	Itanium Processor Family/PA
B3835DA	ProcessResource	Process Resource Manager	No	Itanium Processor Family
B7697BA	ProcessResource	PRM Lib	No	Itanium Processor Family
B8324BA	ServGuardAPI	Cluster Object Manager	No	Itanium Processor Family
T1859BA	ServGuardOPS	ServiceGuard Extension for RAC	No	Itanium Processor Family
B3935DA	ServiceGuard	MC/ServiceGuard	No	Itanium Processor Family
B4580AA	STK	Software Transition Kit	No	Itanium Processor Family
B5139DA	Toolkits	ECM Toolkit	No	Itanium Processor Family
B9116AA	VxVM	Base VERITAS Volume Manager for HP-UX	No	Itanium Processor Family

Product Number	Product Name	Description	Part of HP-UX 11i Version 1.6 Operating Environment	Mode
B6859AA	Webtop	WTSharedX	No	PA
B6865AA	Webtop	Audio Clients	No	PA
J2793B	X25	X.25	No	PA

HP-UX 11i version 1.6 Exclusive Functionality

The following functionality is new functionality which is exclusive to version 1.6 and Itanium. This functionality will not be available for HP-UX 11i on PA-RISC until HP-UX 11i version 2.

MxN threads
14 more dynamically tuneable kernel parameters

MxN thread capability allows multiple kernel threads per user thread and multiple user threads per kernel thread. As such, MxN threading capability allows for a much higher level of threading which can result in much higher performance for Java applications which typically use a high level of threading.

Dynamically tuneable kernel parameters were first introduced with HP-UX 11i in mid-2000. In HP-UX 11i a total of 11 high impact kernel parameters were made dynamically tuneable. This meant that these parameters could be changed dynamically and that a system reboot was not required to have the changes take effect. With HP-UX 11i version 1.5 an additional 14 kernel parameters were made dynamically tuneable.

What is not in HP-UX 11i version 1.6 Release

HP-UX 11i version 1.6 enjoys very wide participation by HP independent software units. The following products are not part of the HP-UX 11i version 1.6 release.

HP-UX Workload Manager
Secure web console
Central web console
HP-UX Virtual Partitions (vPars)
iCOD
Autoport Aggregation
MetroClusters
ContinentalClusters
System Configuration Repository (however, this is replaced by System Inventory Manager which will be available for HP-UX 11i Version 1.6 from Software Depot)
Netscape Directory Server
LDAP-UX Integration

HP-UX Kerberos Server
HP-UX Secure Shell
HP-UX AAA Server

Current plans call for all of these products or products with equivalent functionality to be supported with HP-UX 11i version 2.

HP-UX 11i version 1.6 Functionality Available on the Web by end of 2002

The following additional independent software units are scheduled to be available for HP-UX 11i version 1.6 on the web by the end of 2002

- Next generation ServiceControl Manager
- WBEM (Web-based Enterprise Management)
- Low Latency HyperFabric (low latency, high bandwidth algorithm in kernel for clustering)
- Java Development Kit 1.3.1.06 (1.3.1.04.1 in 11.22 Release)
- Java Plug-In 1.3.1.06
- Java 1.3.1.06 Runtime Environment
- Java 3D for 1.3/1.4
- Java Development Kit 1.4
- Java Plug-In 1.4
- Java 1.4 Runtime Environment
- IP filter
- IPSec
- ServiceGuard/MC for NFS
- Opensource tools (autoconf, automake, bash, binutils, bison, ddd, emacs, flex, freetype, gettext, glib, gtk+, gzip, imagemagick, imake, ipeg, libiconv, libpng, m4, make, mesa, openssh, openssl, patch, pine, qt, readline, sendmail, sudo, tar, tcl, tcsh, tesinfo, tiff, tk, unzip, vim, xemacs, xpdf, xpm, yamm, zip, zlib)

Functionality Differences in the HP-UX 11i version 2 Timeframe

HP-UX 11i version 2 is due to be released in mid-2003. HP-UX 11i version 2 will be a joint release for both the Itanium PA-RISC architectures. In this timeframe the plans call for HP-UX 11i and its layered products to provide equivalent functionality on both the PA-RISC and Itanium architectures with vPars as the major difference.

HP Support Services Available for Itanium processor family systems

HP offers an extensive suite of services for the Itanium Server and workstation families. These services were developed to meet customer needs, including Planning; Porting & Migration; Implementation; Support (for both the hardware and the operating system); Education and Finance.

The HP services for Itanium include the following:

- Consulting & Integration, Transition Analysis, Security Consulting & Analysis and Data Migration
- Free Porting and Migration Assessment; Fix-Price detailed assessment; Porting & Migration Solution Delivery
- Migration Planning & Review, onsite system installation, SSL web server (for HP-UX and Linux); Support offerings for hardware and the Operating System of choice
- A full plethora of courses, including a variety of Web-based courses focused on Itanium
- Financing programs for customers and channel partners

Summary and Conclusion

An evolutionary revolution has begun, powered by the architectural innovation of HP Labs and the manufacturing prowess of Intel Corporation. The result of this collaboration, the Itanium architecture, will change computing as we know it and will thereby change the world.

HP-UX 11i was the first operating system to support the new architecture and is acknowledged to be the only enterprise quality operating system on the Itanium architecture. HP-UX 11i offers the easiest path in the history of computing to a new architecture. HP-UX 11i customers will experience minimal disruption moving from PA-RISC to Itanium as a result of careful planning by HP. HP-UX 11i customers will experience a small speed bump while customers of other vendors will see a yawning and daunting chasm that they must cross.