Integrity Server Products and Futures

Ric Lewis

Director, Product Planning and Strategy

Business Critical Systems

Hewlett-Packard

Agenda

- Integrity/Itanium Strategy
- PA-Risc & Alpha Transition
- Integrity Product Lineup
- Integrity Platform Futures

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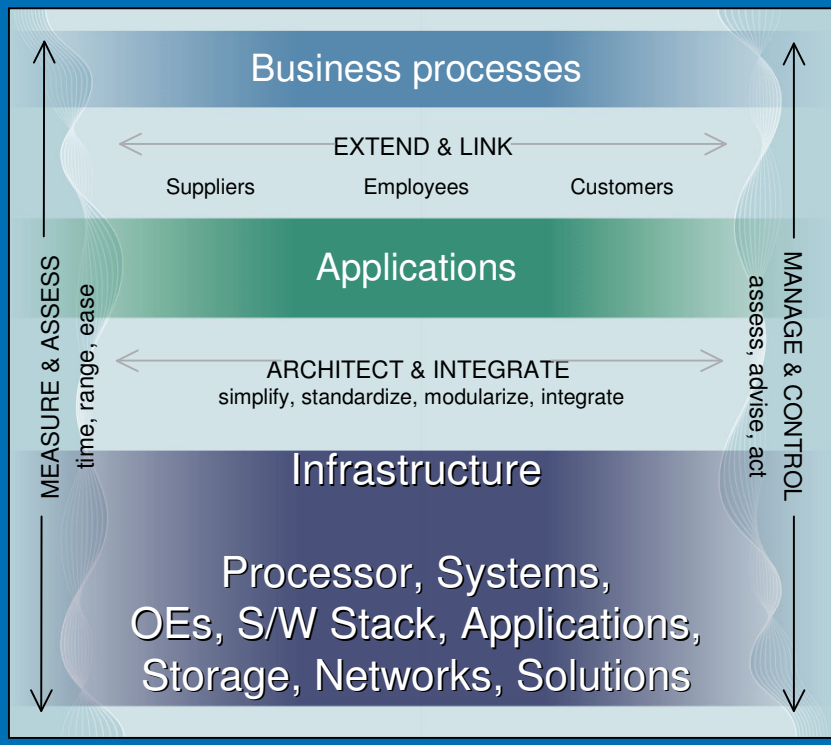
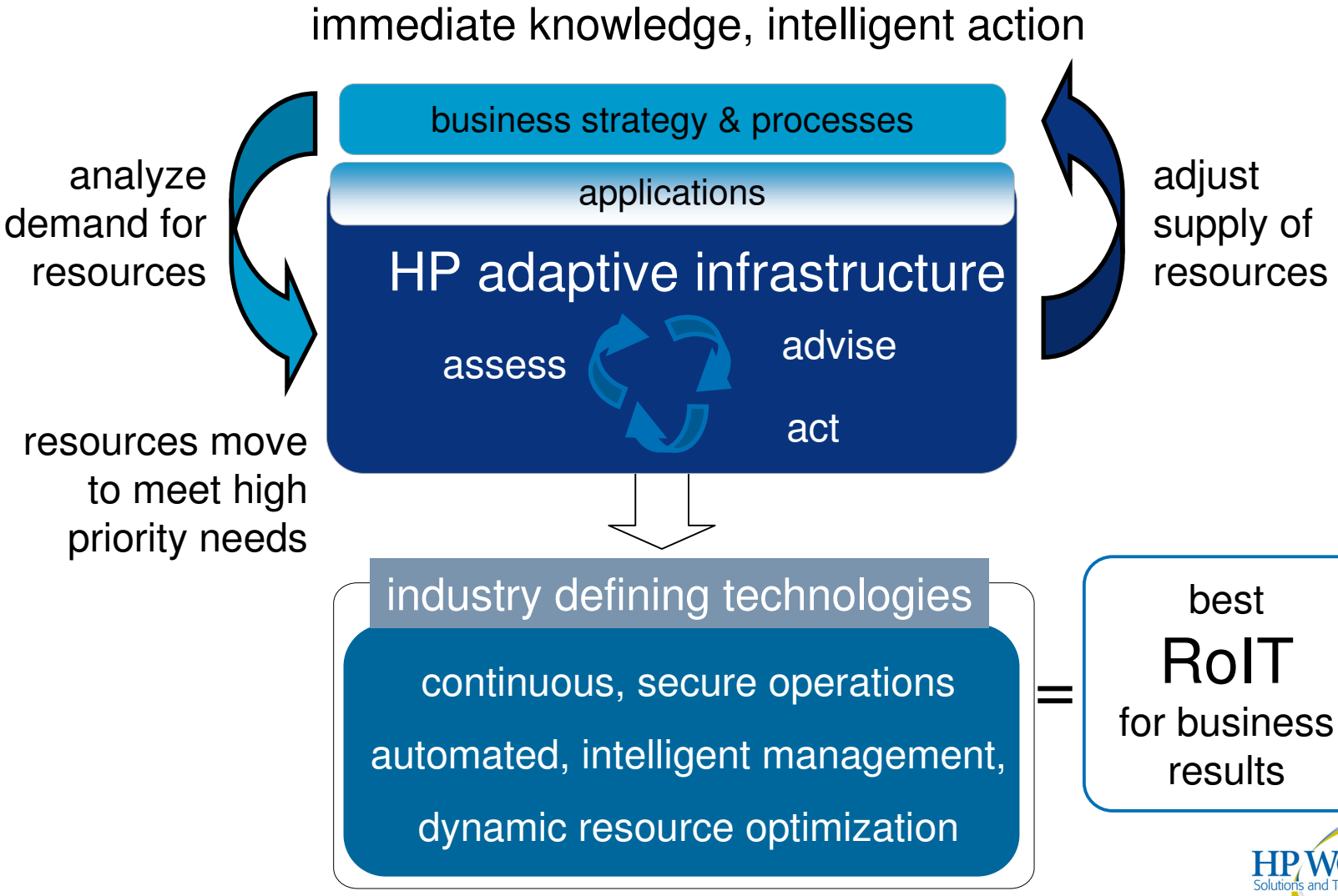
The next big thing

Adaptive Enterprise
= Business and IT Synchronized to Capitalize on Change

+ Standards Based Computing
+ Multi-OS
+ Flexible, Adaptable, Reliable
+ Management Simplicity
+ Dynamic Allocation of Virtualized Resources to Changing Work Loads
+ Utility Pay-per-use Business Model



Business agility requires an HP adaptive infrastructure

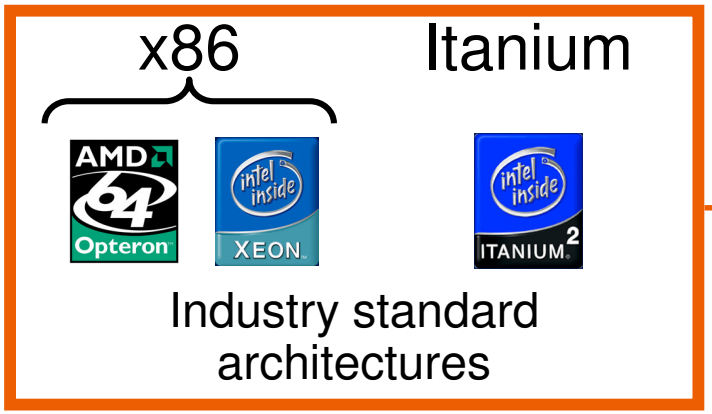


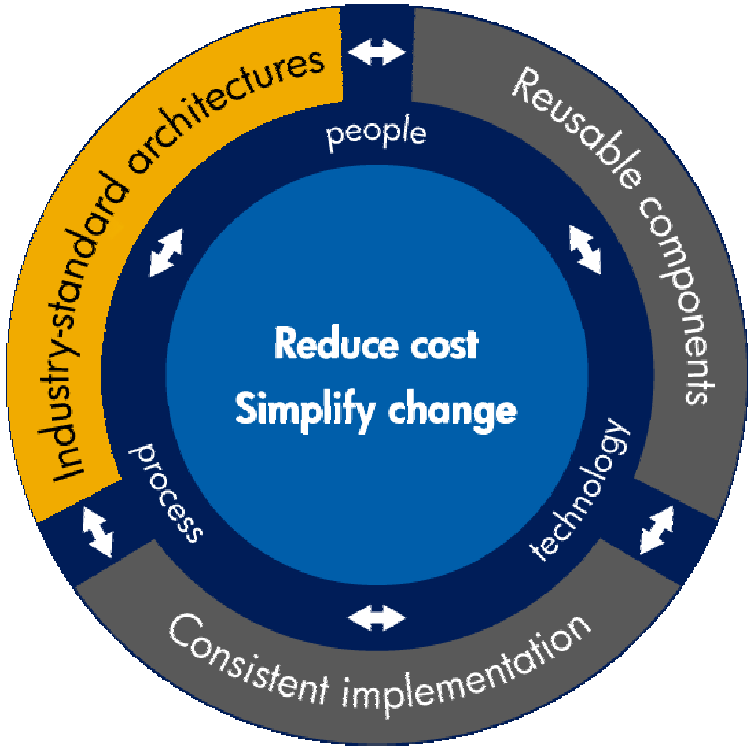
An Adaptive Enterprise Starts with Standards

HP is:

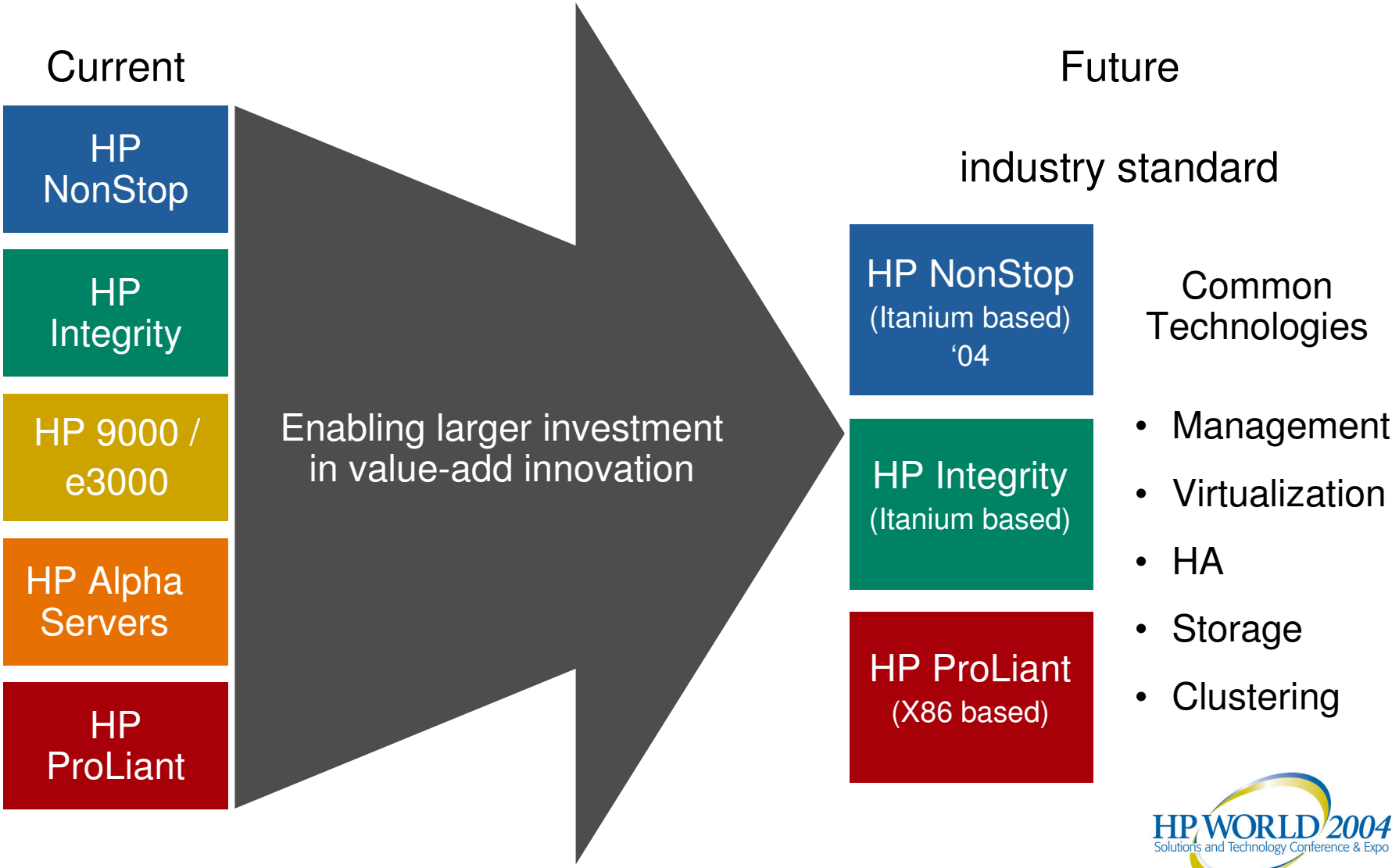
- Committed to providing the best in industry standard components
- Providing more customer choice without compromise
- Investing in industry standards and focused innovation

Complementary, modular approach based on two standard architectures

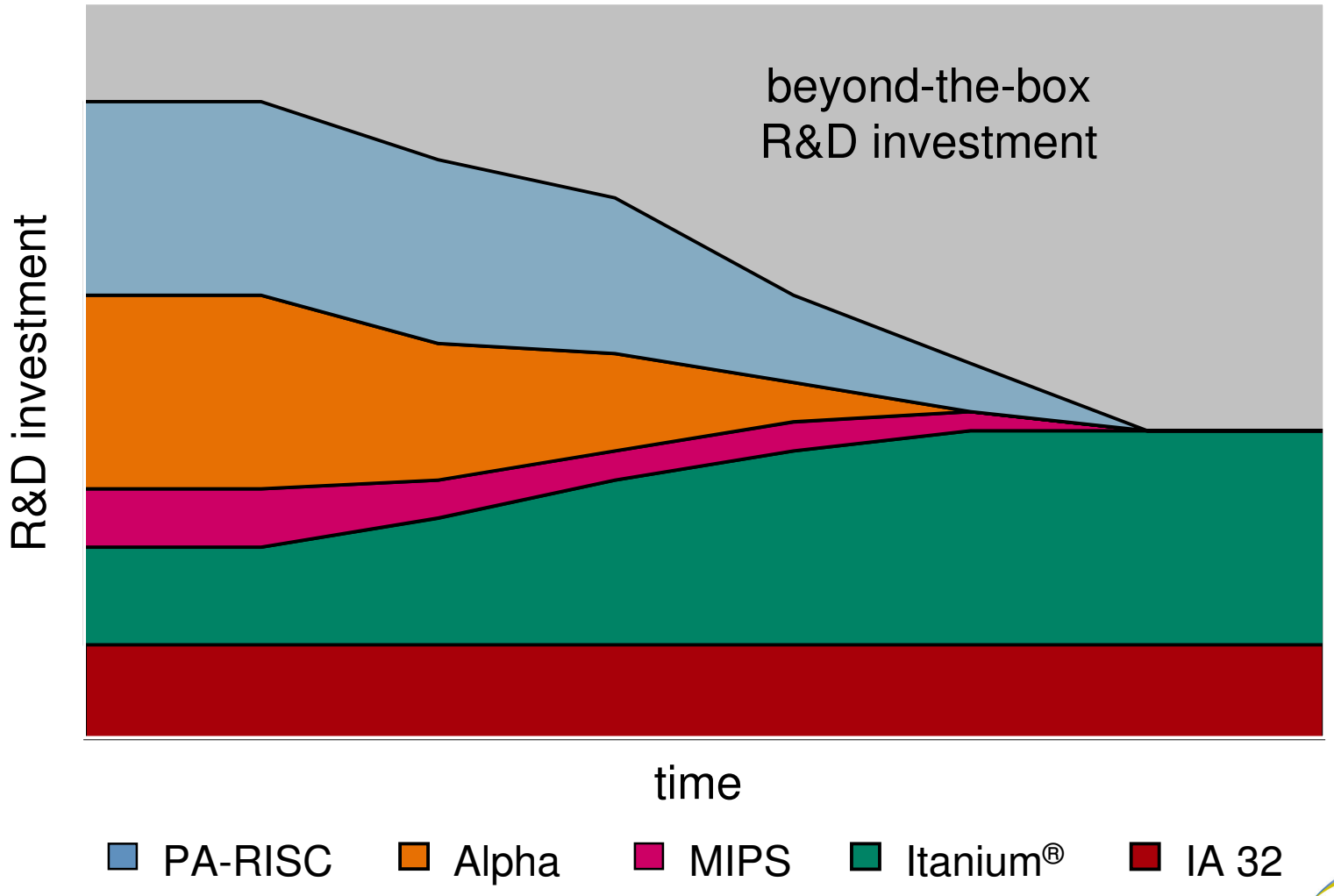




Moving to 3 leadership product lines – built on 2 industry standard architectures



Investing beyond the box
Focused innovation



Why a “Standards” Approach?

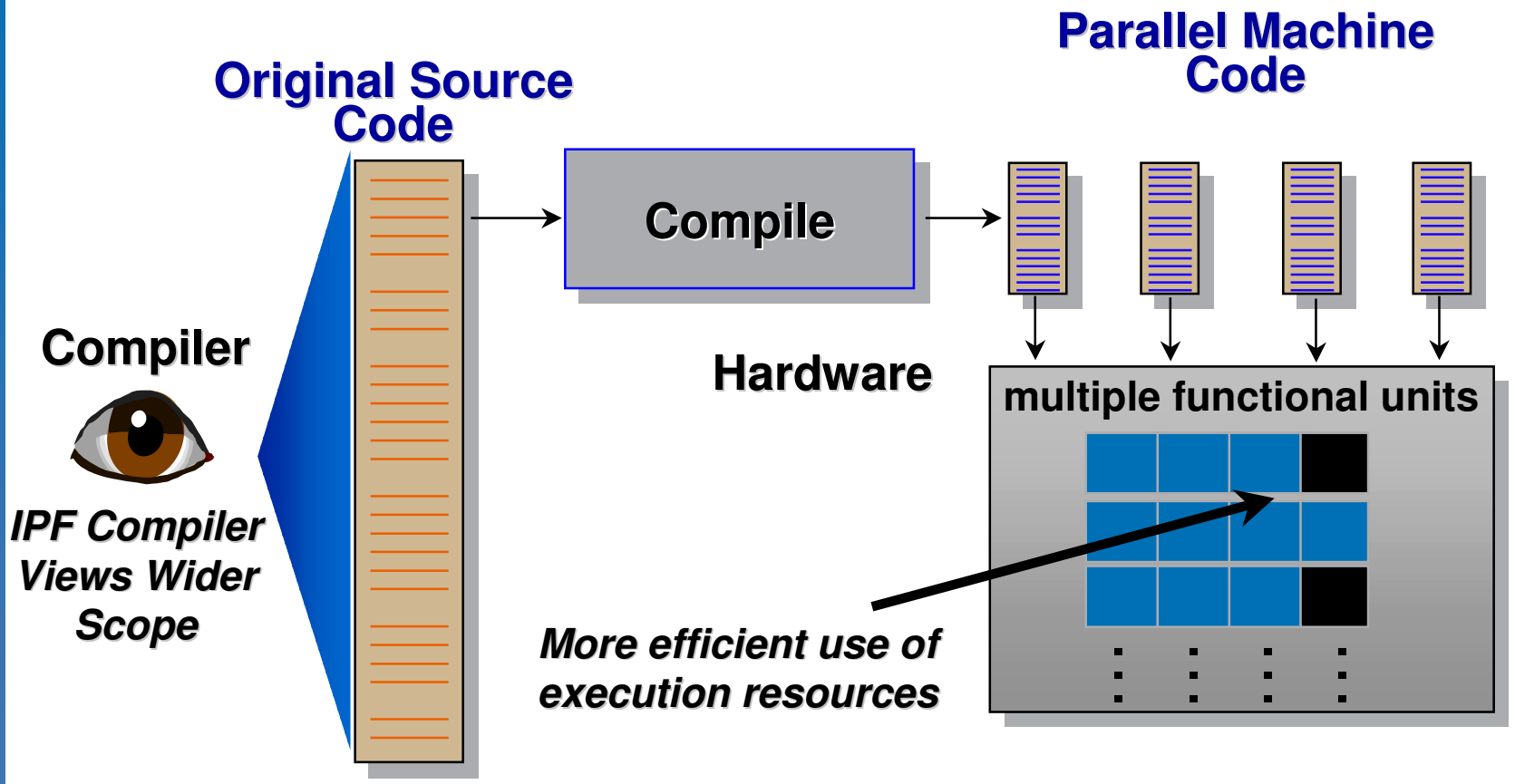
EPIC → Intel Itanium

- Moore’s 2nd Law ➔ Fab Economics
- Customer Contribution / Market Trends
  - Shift in Investment Focus
- Flexibility of multi-OS, vs. Single Use Platform
- Enables partnering to create best-in-class solutions
- Drives leadership cost structures

Why a New Architecture?

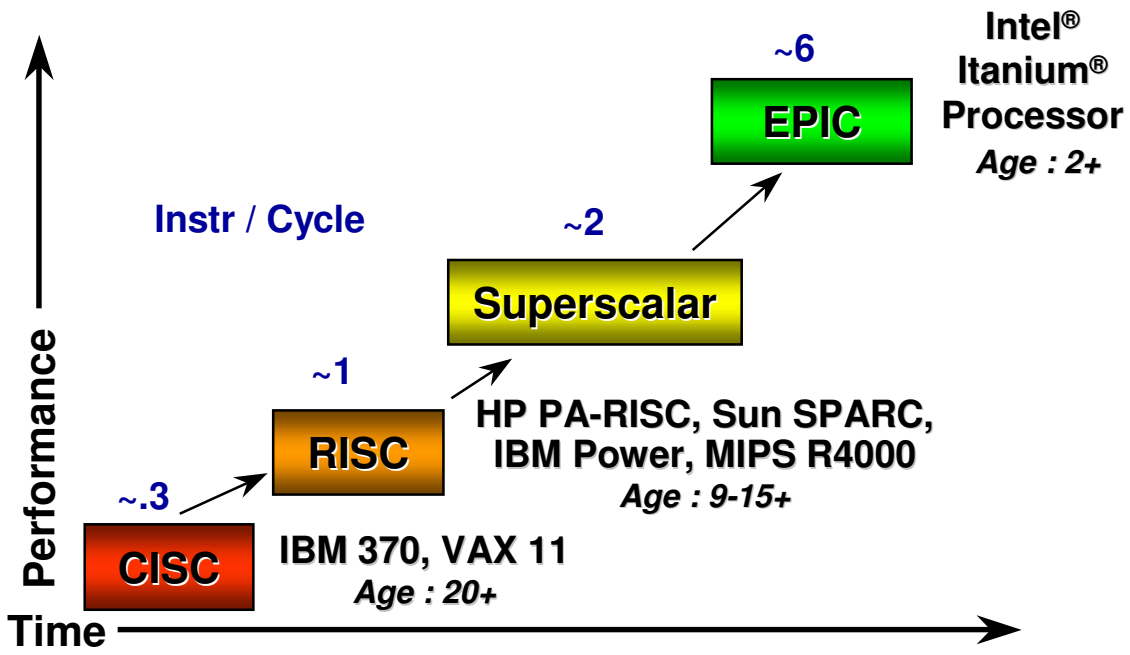
- New workloads relentlessly demand greater application performance, at lower price/performance
- The need to overcome the limitations of RISC
  - RISC (and CISC) architectures based on Von Neumann model; processing must appear to be done sequentially
  - Exponential increase in logical control complexity of Out-of-Order processing
  - Increased circuit overhead to take RISC to greater levels of parallel execution not economical (cost increase > performance increase)
- Recognize that for processor architecture to sustain execution of multiple instructions per cycle, compiler must explicitly schedule instructions
- Requirement for much greater number of architected registers to expose the parallelism
- Increasing demand on processor fault management and scalability to meet the needs of enterprise data centers

Itanium/EPIC Architecture: Explicit Parallelism



Increases Parallel Execution

Intel Itanium Architecture: Designed for Business Critical Computing



Next Enterprise Architecture

Larger and more demanding workloads require new approach:

- Designed for 64-bits from the ground up
- Architected for performance, scalability, and business critical availability

Performance through parallelism

- Built-in instruction-level parallelism
- Issue ports and execution units support up to twice as many instrs/clock cycle
- Maturity curve narrows clock speed gap over time

Massive on-chip resources

- 128 general registers, 128 floating point registers, 8 branch ((vs 16 on x86)
- Fewer memory accesses (loads/stores) on complex workloads

Beating the memory latency gap & shorter pipeline

- Very large virtual and physical address spaces
- Shorter memory pipeline
- Latency avoidance
- Predication of instruction execution
- Data and control speculation

Business Critical Availability

- Machine Check Architecture
- Security: sophisticated ring protection and buffer overflow protection
- Protected data paths
- Failure mode analysis

Architecture Success Factors

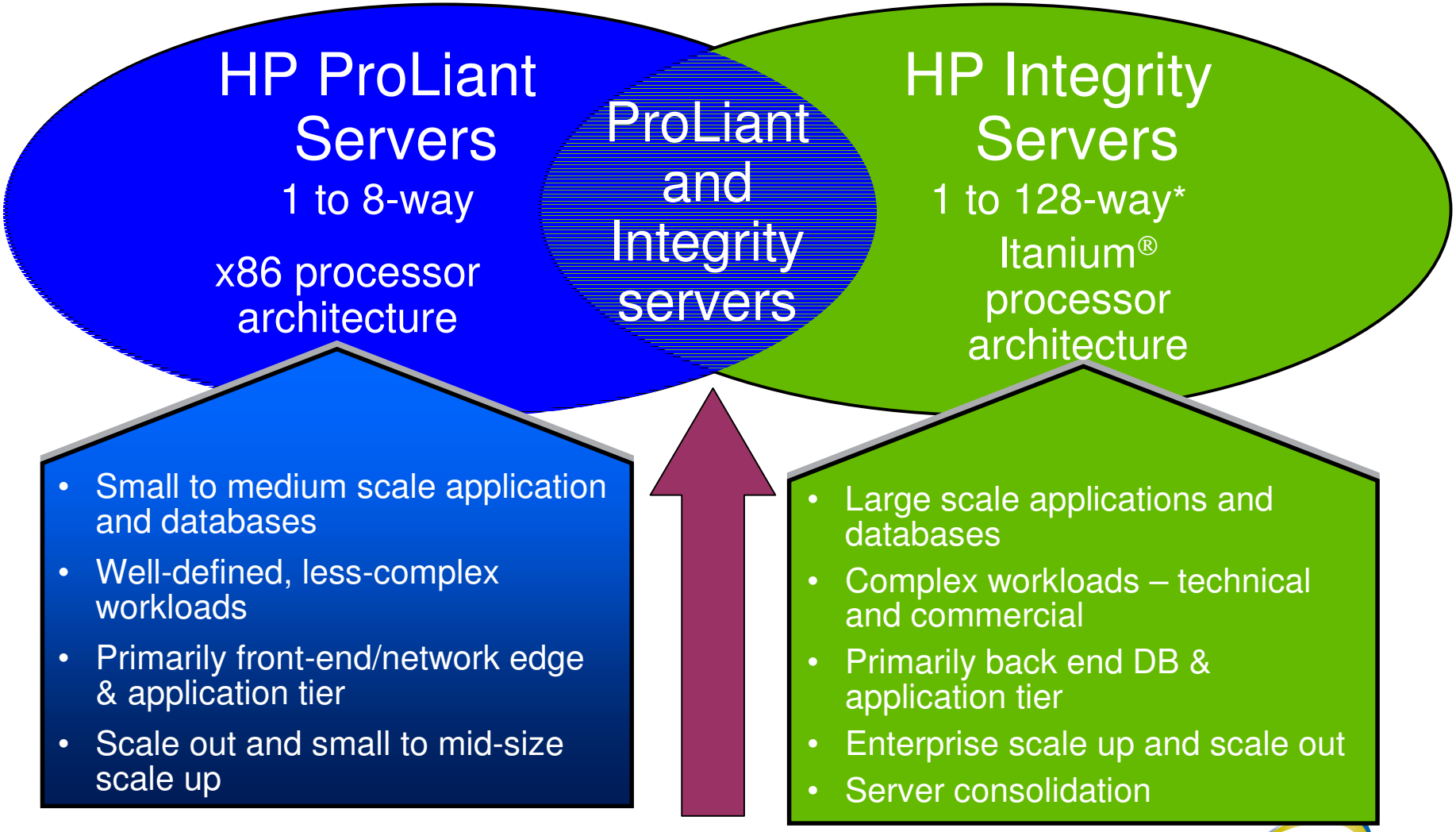
Success Factors	Status

- **Technology** :
  - Semiconductor manufacturing
  - Architecture
  - Design
	Combination of investment and capability unmatched in the industry

- **Economics**	Standards approach drives volume and cost, leverages best-in-class solutions, enables partnership / collaboration

- **Industry Adoption**
  - Applications
  - Systems (wide range low to high end)
  - Industry ecosystem
  - Supply chain
  - Supporting technology
	>2200 apps today, rate of new apps increasing; ~40+ systems from 10 server suppliers (every major company except Sun); Expect Itanium proc volume > any RISC in '05-'06.

Customer choice



Customer-specific needs driven

* Future

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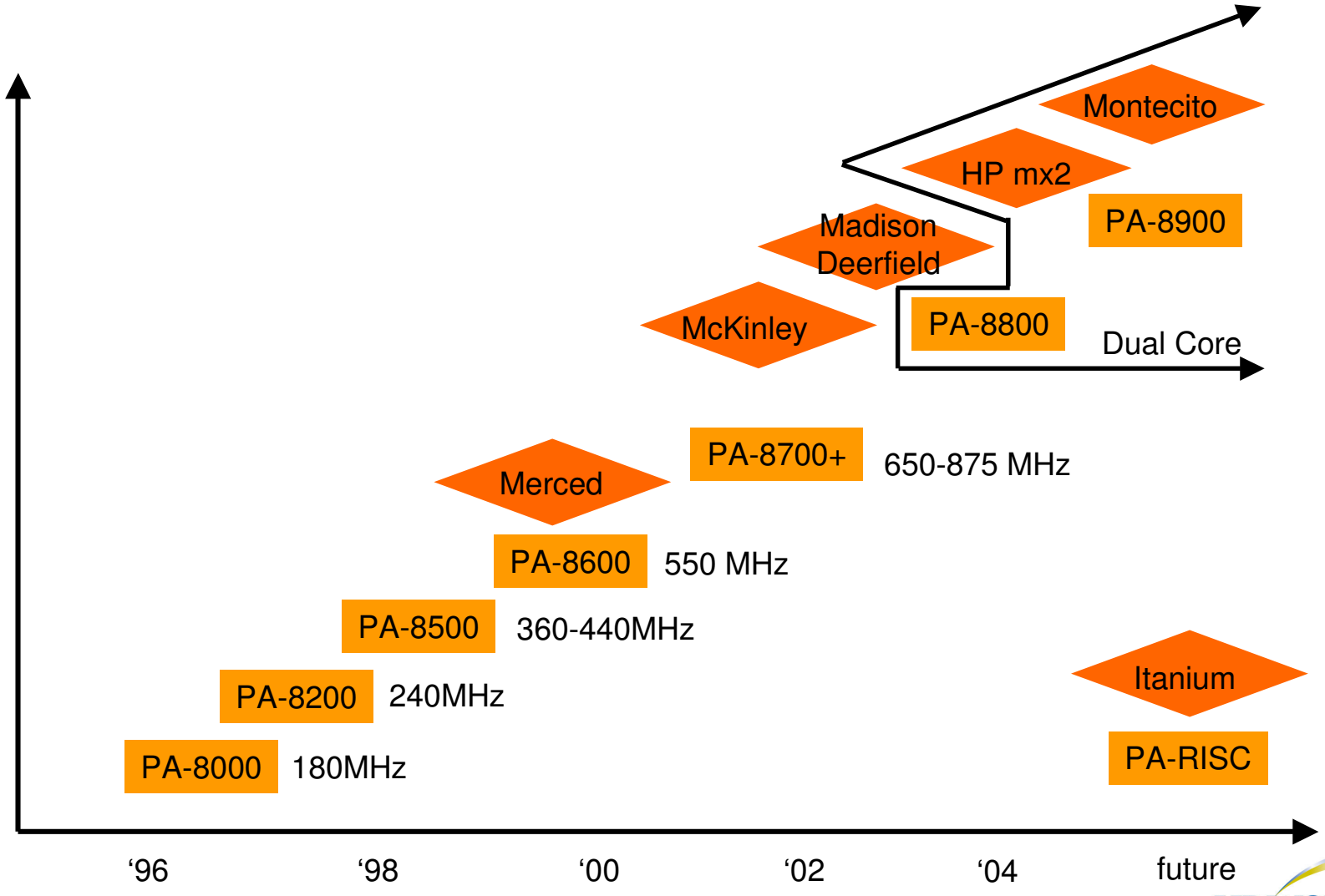
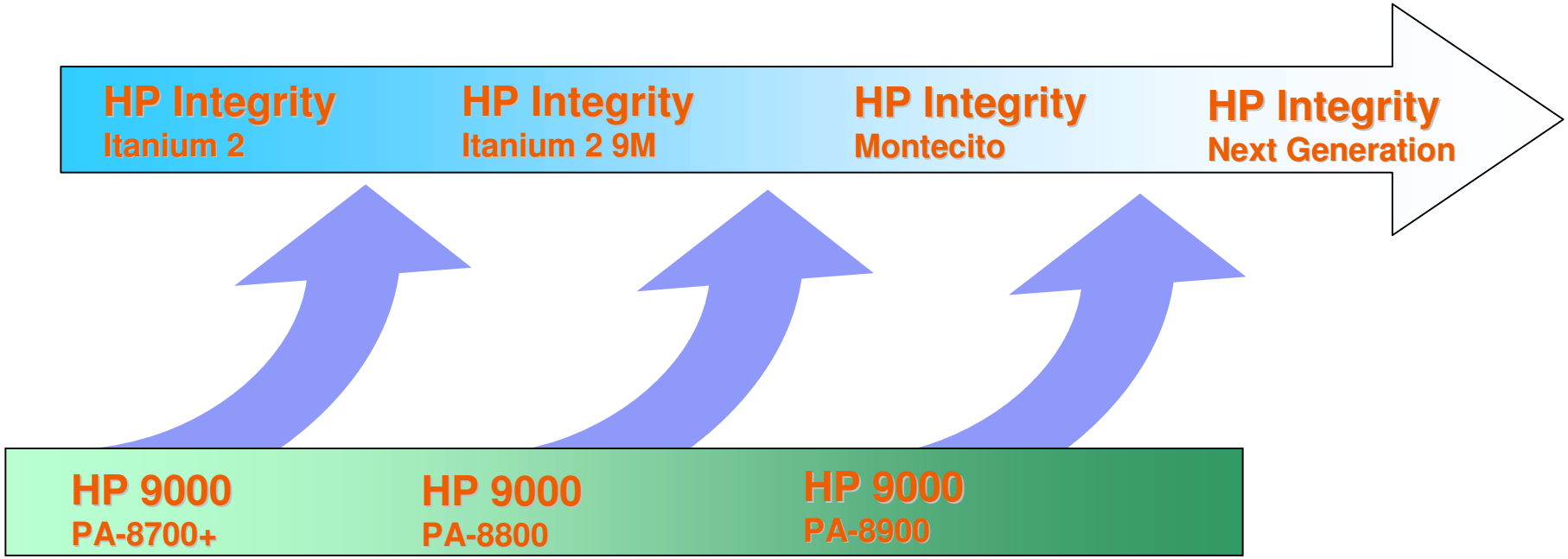
Microprocessor Roadmap
PA-RISC and Itanium



HP 9000 to Integrity migration



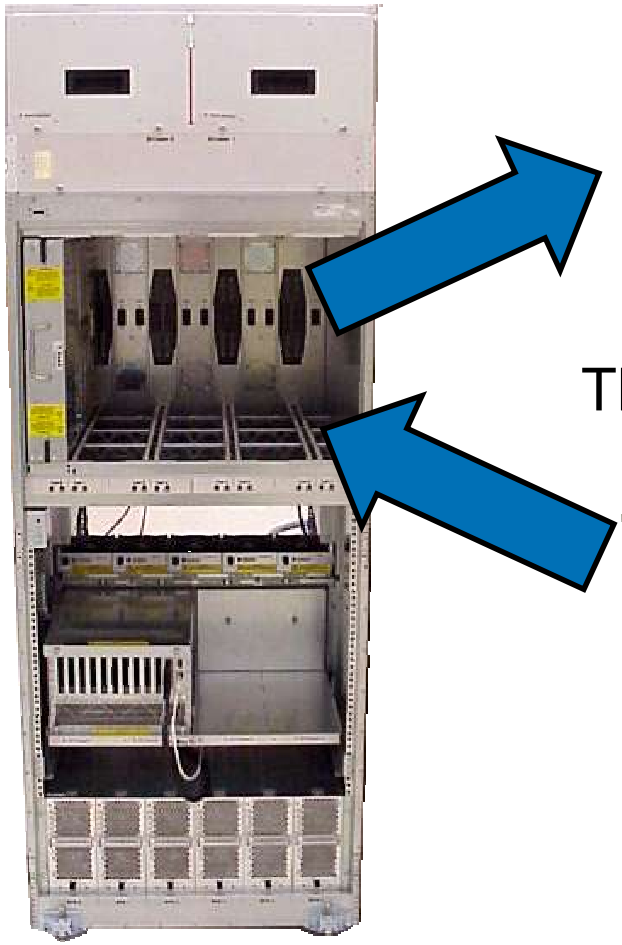
- Customers pick the time that is right for them
- Simple evolution (In-box upgrades)
- Superior investment protection
- Tools, partners & services available to help customers evolve

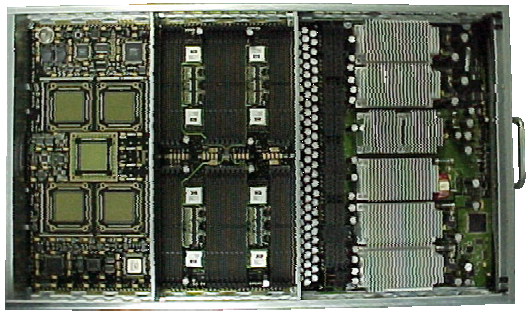
PA leverage from Itanium simplifies transition

- HP's relationship with Intel allowed us to leverage the Itanium CPU bus and form factor for PA-RISC

- HP first implemented this standard with the PA-8800
  - Allows HP to develop one set of chipsets, boards, and systems for both architectures
  - Makes it extremely simple to switch architectures
    - Simply remove the PA CPUs from the boards, replace with Itanium CPUs, and flash the firmware.
    - Nothing else in the system changes (boards, chassis, memory, power, cooling, manageability, etc.)

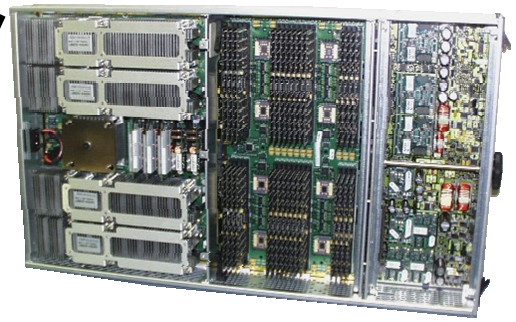
Cell board swap converts from PA8600-8700+ to PA-8800/8900, and all Itanium® CPUs





Superdome "Yosemite" cell board for PA 8600, 8700, and 8700+

The same (existing) chassis is used for all products.

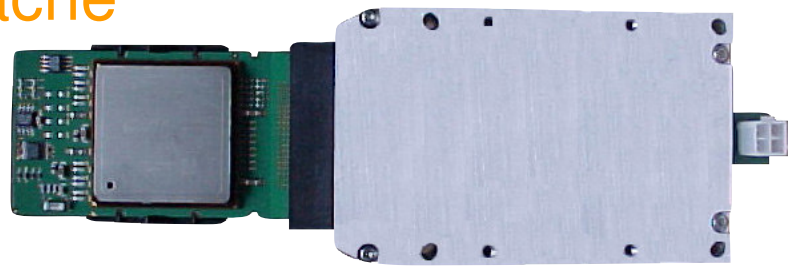


Superdome "Pinnacles" cell board for PA 8800, 8900, and all Itanium® processors

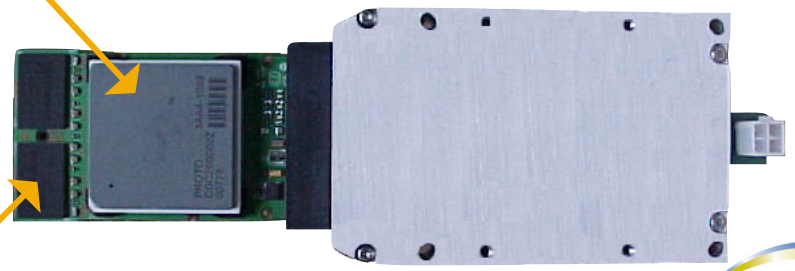
Superdome is shown, but an identical path exists for the rp8400 and rp7410.

PA leverage from Itanium simplifies transition

Itanium2 ® CPU module from Intel containing one CPU core and up to 6MB of on-chip cache



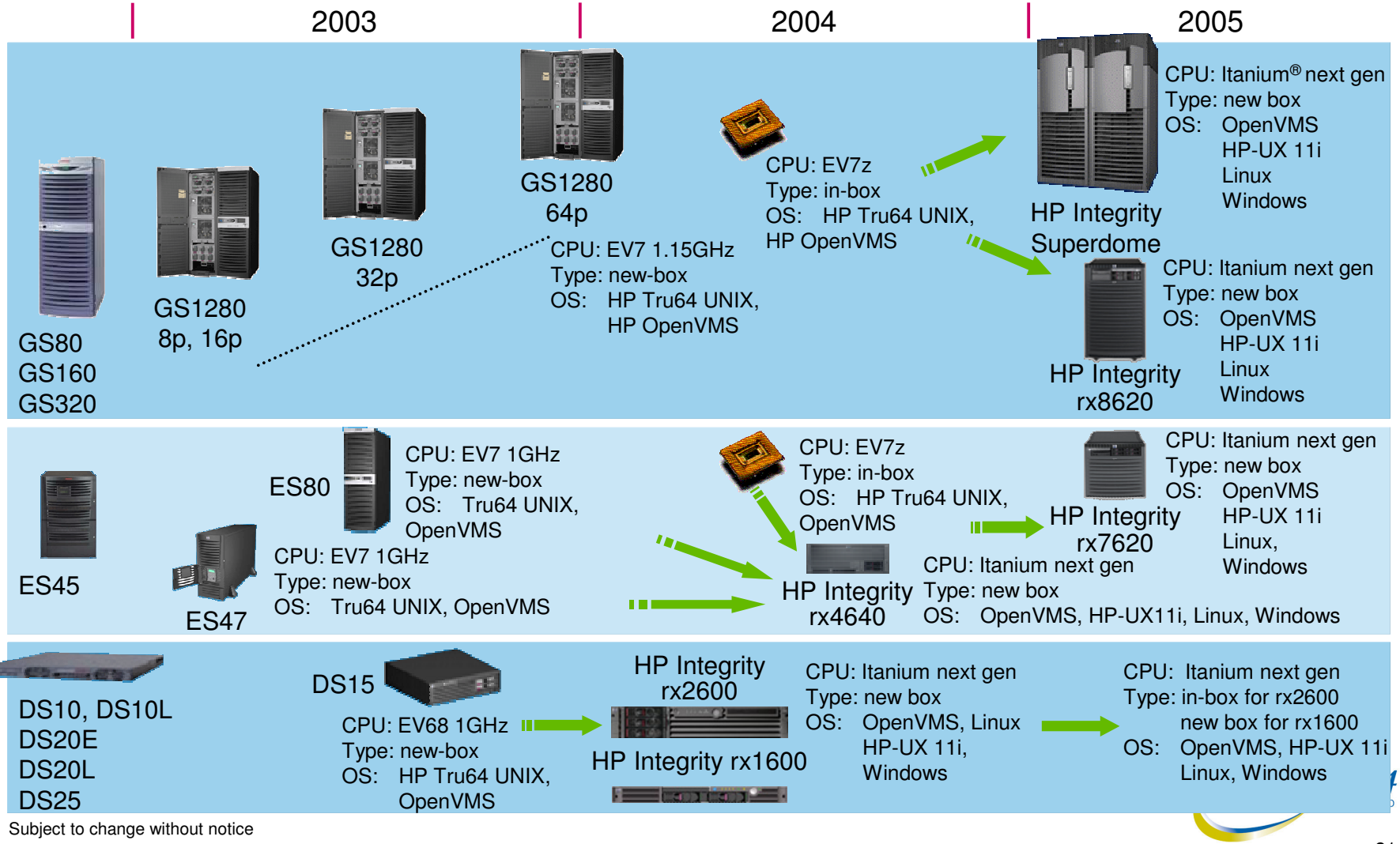
PA-8800 CPU module from HP containing two CPU cores, 3MB of on-chip cache, and 32MB of off-chip cache



32MB of off-chip cache

HP AlphaServer evolution

Sales at least until 2006, with support at least until 2011



Subject to change without notice

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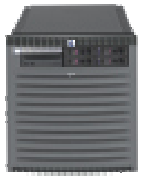
HP Integrity servers

Max. CPUs

64	HP Integrity Superdome		**Up to 64-way scalability and hard partitioning capability for leading consolidation**
16	HP Integrity rx8620		**16-way scalability and hard partitioning capability for consolidation**
8	HP Integrity rx7620		**8-way flexibility with high performance, density, and partitioning capabilities**
4	HP Integrity rx4640		**4-way high-performance servers in ultra-dense and highly scalable models**
2	HP Integrity rx2600 & rx1600	 	**2-way ultra-dense, power-packed server redefines entry-level computing**

- **Up to 64 Intel® Itanium® 2 processors**
- **Up to 512 GB memory**
- **192 PCI-X slots (with SEU)**
- **Up to 16 hard partitions**

- **2- to 16-way Intel Itanium 2 processors**
- **Up to 128 GB memory**
- **32 PCI-X slots (with SEU)**
- **Up to 4 hard partitions**
- **2 servers per 2m rack**

- **2- to 8-way Intel Itanium 2 processors**
- **Up to 64 GB memory**
- **15 PCI-X slots**
- **Up to 2 hard partitions**
- **4 servers per 2m rack**

- **1- to 4-way Intel Itanium 2 processors**
- **Up to 64 and 96 GB memory**
- **6 and 10 PCI-X slots**
- **10 and 5 servers per 2m rack**

- **1- to 2-way Intel Itanium 2 processors**
- **Up to 24 GB memory**
- **4 PCI-X slots**
- **20 servers per 2m rack**

Windows Server 2003 OpenVMS HP-UX 11i Version 2

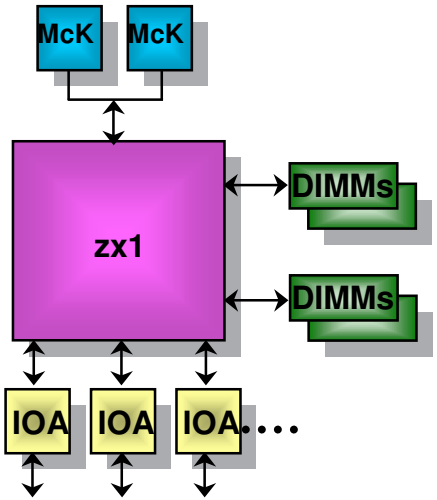
HP zx1 chipset

1-2 Way Configuration

System Bus
128 bits wide
200MHz/400 MT/s
6.4 GB/s

Memory
266 Mhz DDR
lowest latency
8.5 GB/s
"chipkill"

IO
4 GB/s
PCI-X/AGP Support

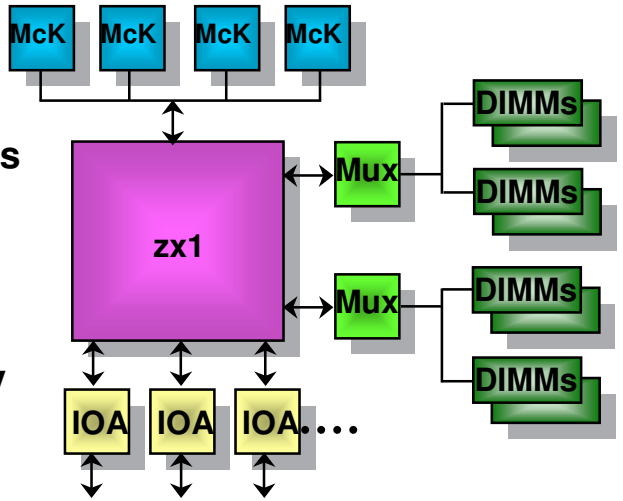


4 Way Configuration

System Bus
128 bits wide
200MHz/400 MT/s
6.4 GB/s

Memory
200 Mhz DDR
highest capacity
12.8 GB/s
"chipkill"

IO
4 GB/s
PCI-X 133Mhz/64bit



HP's zx1 chipset delivers industry leading memory latency and bandwidth, I/O capability, and resilience features for Intel's Itanium2 processor family

rx1600

- One or two Itanium2 processors
  - Deerfield low-voltage, low-power CPUs
- 2 independent PCI-X slots

- 200 MHz processor bus
  - 6.4 GB/s of bandwidth
- Advanced memory technology
  - 8 memory DIMM slots for DDR SDRAM
  - 16 GB of memory
- System Package
  - 1U, 27 inches deep
  - 2 hot-swap bays for 1” hard disks, 1 built-in DVD ROM
  - built-in dual lan

rx2600

- 2 CPU sockets
  - 2 way Itanium2 Madison (rx2600)
- 4 independent PCI-X slots

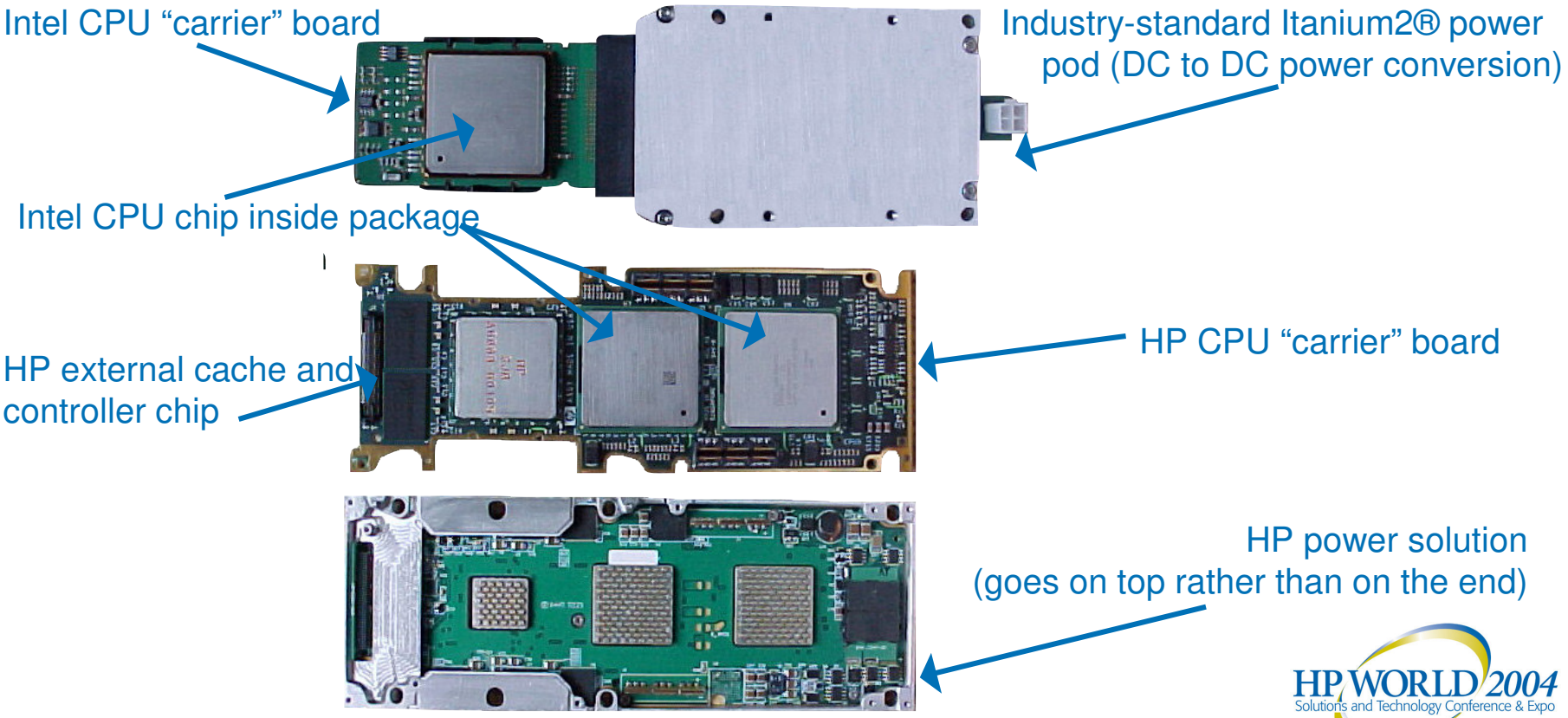
- 200 MHz processor bus
  - 6.4 GB/s of bandwidth
- Advanced memory technology
  - 12 memory DIMM slots → 24GB of memory
  - 8.5 GB/s of memory bandwidth (peak)
  - “chipkill” multi-bit memory error correction
- System Package
  - 2U, 26 inches deep
  - 3 hot-swap bays for 1” hard disks, 1 built-in DVD ROM
  - Optional redundant power supplies and cords

rx4640

- 4 CPU sockets
  - 4 way Itanium2 Madison (rx4640)
  - 8 way Itanium2 mx2 module
- HP zx1 chipset
  - 12.8 GB/s of memory bandwidth
  - “chipkill” multi-bit memory error correction
- Offered with 16 or 32 DDR DIMM slots
  - 1GB and 2GB DIMMs available
- System Package
  - 19” rack, 4U form factor → 2X density over existing rx5670
  - 2 hot-swap bays for 1” hard disks, built-in DVD ROM and LS-240 drive
  - Optional redundant power supplies and cords

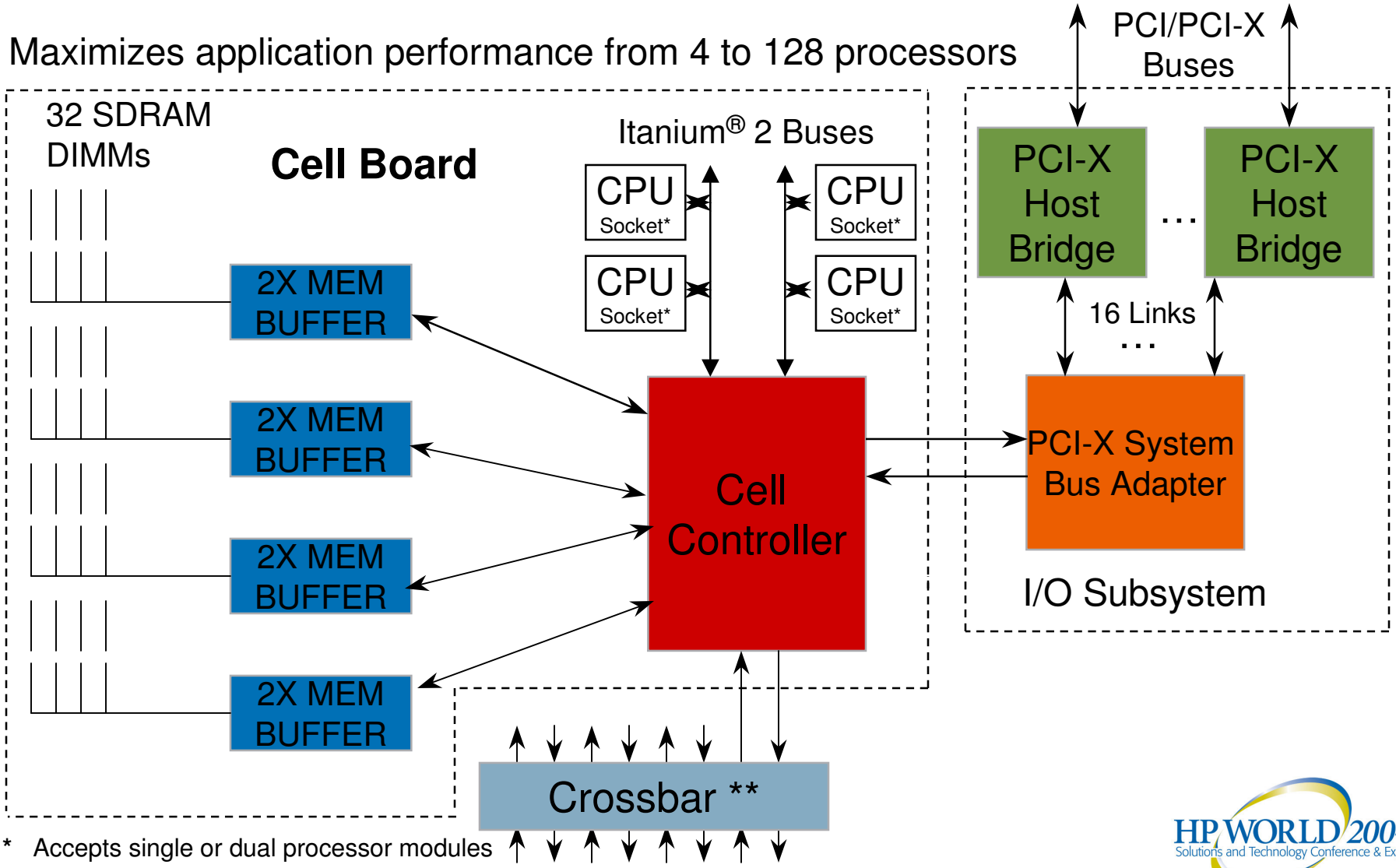
“Inventing” a dual core Itanium® CPU

- The standard Intel cartridge packaging is not at maximum density
  - CPU silicon chip is in a package, on a carrier board, with power on the end
  - The basic chip and package could be packed much more densely



sx1000 chipset for hp's mid-range and high end systems

Maximizes application performance from 4 to 128 processors

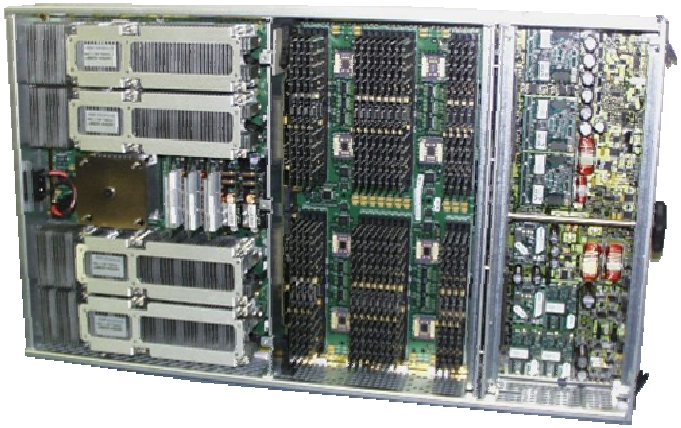


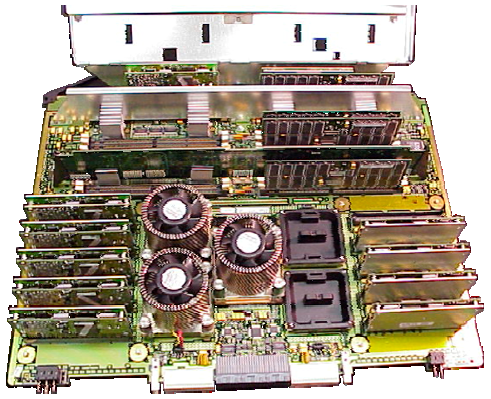
* Accepts single or dual processor modules

** Not used in 8 socket systems

Cell Boards

- 4 processor sockets
  - 2 CPU busses
- 8 or 12 I/O slots per cell
  - PCI-X (1 GB/s bandwidth)
  - Each slot is its own PCI-X bus
- Memory technology
  - 16 or 32 DIMM sites
  - “chipkill” multi-bit error correction
- Cache Coherent Interconnect
  - Connects to other cells to form partitions





rx7620

- 8 CPU sockets
  - 8 way Itanium2 Madison (rx7620)
  - 16 way Itanium2 mx2 module

- Same cellular technology as Superdome
  - Performance, partitioning, etc.
  - 32 DIMM slots → 64 GB of memory
  - “chipkill” multi-bit error correction
  - 16 PCI I/O slots

- System Package
  - 10U, 28.5 inches deep
  - 4 hot-swap hard disks bays, 1 removable media bay
  - 2N redundant power supplies
  - Optional redundant power cords

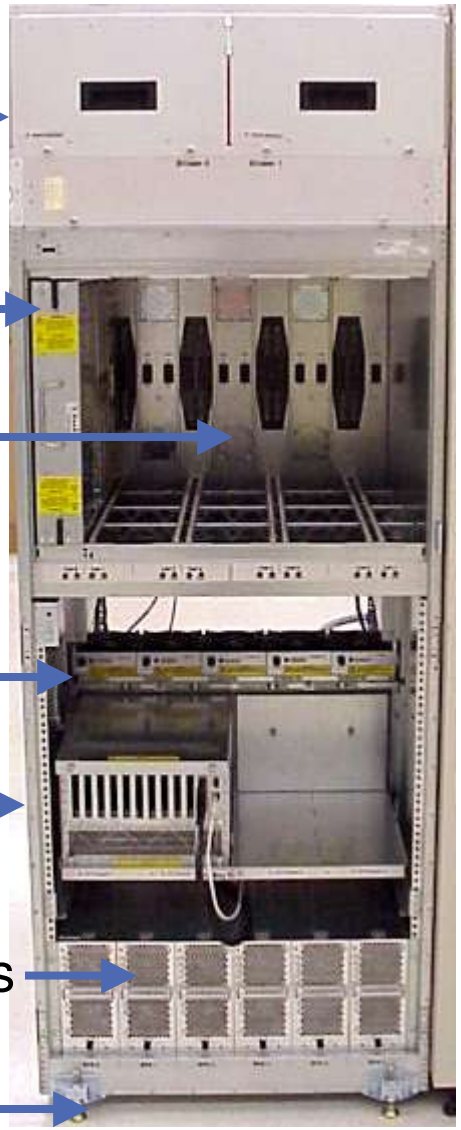
rx8620

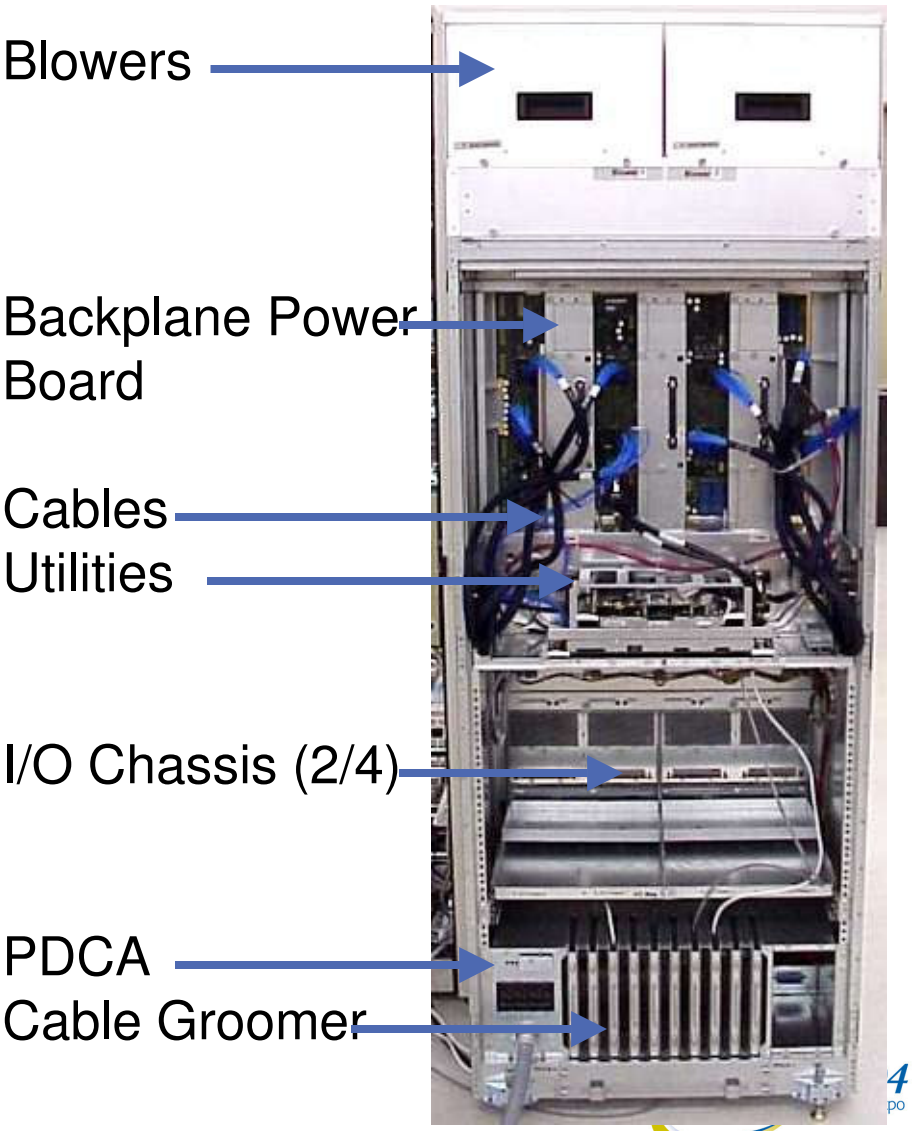
- 16 CPU sockets
  - 16 way Itanium2 Madison (rx8620)
  - 32 way Itanium2 mx2 module
- Same cellular technology as Superdome
  - Performance, partitioning, etc.
  - 64 DIMM slots → 128 GB of memory
  - “chipkill” multi-bit error correction
  - 16 PCI I/O slots
- System Package
  - 17U, 28.5 inches deep
  - 4 hot-swap hard disks bays, 2 removable media bays
  - N+1 redundant power supplies
  - Optional redundant power cords
- Optional I/O expander
  - 16 additional PCI I/O slots
  - 4 more hot-swap disks and 2 more removable media bays

Superdome

- 64 CPU sockets
  - 64 way Itanium2 Madison (dual cabinet)
  - 128 way Itanium2 mx2 module
- sx1000 chipset technology
  - 512 DIMM slots → up to 1 TB of memory
  - “chipkill” multi-bit error correction
  - Hard partitioning
  - Up to 192 PCI-X I/O slots
- System Package
  - Custom cabinet
  - N+1 redundant power supplies
  - Optional redundant power cords

Superdome System View





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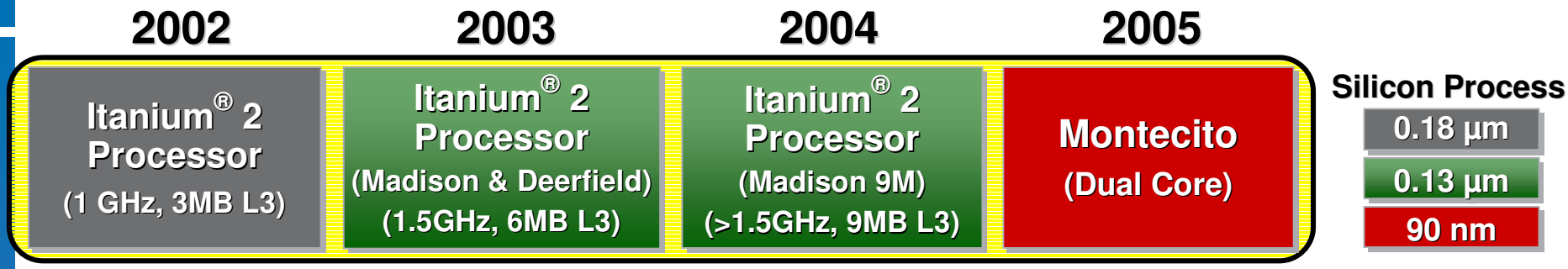
Itanium® Processor Family Roadmap



- **Itanium® 2 Processor (Madison) – shipping across entire product line**
- **Itanium® 2 platform maintains same socket, bus and software compatibility**
- **Intel will enhance Itanium® 2 processor (Madison) with larger 9M L3 cache**
- **Montecito processor will enable dual-core technology and enhanced micro-architecture**

Roadmap maintains world class performance

HP Integrity and HP 9000 Server Roadmap

Revision 4.5 July-04

	Current offering	2004	2005	2006
 4-128P	HP 9000 Superdome		CPU: PA-8900 (dual-CPU) OS: HP-UX 11iv1, v2, v3*	New Chipset CPU: PA-8900 OS: HP-UX 11iv1, v2, v3 DDR-II
	HP Integrity Superdome	CPU: mx2 module OS: HP-UX11iv2, Windows CPU: Itanium2 9M OS: HP-UX11iv2, Windows, Linux*	CPU: Itanium2 "Montecito" New Chipset OS: HP-UX 11iv2, v3* Windows, Linux, OpenVMS DDR-II	PCI-E
 2-16P 2-32P	HP 9000 rp7410-8, rp8400-16 rp7420-16, rp8420-32		CPU: PA-8900 (dual-CPU) OS: HP-UX 11iv1, v2, & v3*	New Chipset CPU: PA-8900 OS: HP-UX 11iv1, v2, v3 DDR-II
	HP Integrity rx7620-16, rx8620-32	CPU: mx2 module OS: HP-UX11iv2, Windows CPU: Itanium2 9M OS: HP-UX11iv2, Windows, Linux*	CPU: Itanium2 "Montecito" New Chipset OS: HP-UX 11iv2, v3* Windows, Linux, OpenVMS DDR-II	PCI-E
 1-8P	HP 9000 rp4440-8		CPU: PA-8900 (dual-CPU) OS: HP-UX 11iv1, v2, v3*	
	HP Integrity rx4640-8	CPU: mx2 module OS: HP-UX11iv2, Windows, OpenVMS* CPU: Itanium2 9M OS: HP-UX11iv2, Windows, Linux*, OpenVMS	CPU: Itanium2 "Montecito" OS: HP-UX 11iv2, v3* Windows, Linux, OpenVMS	New 8p Server & Chipset CPU: Itanium2 "Montecito" OS: HP-UX, Windows, Linux, OpenVMS DDR-II PCI-E
 1-4P	HP 9000 rp3440-4		CPU: PA-8900 (dual-CPU) OS: HP-UX 11iv1, v2, v3*	
	HP Integrity rx2600-2	CPU: Itanium2 9M OS: HP-UX11iv2, Windows, Linux* OpenVMS	CPU: Itanium2 "Montecito" OS: HP-UX 11iv2, v3* Windows, Linux, OpenVMS	New 4p Server & Chipset CPU: Itanium2 "Montecito" OS: HP-UX, Windows, Linux, OpenVMS DDR-II PCI-E
 1-2P	HP Integrity rx1600-2		CPU: Low voltage Itanium2 (+) OS: HP-UX 11iv2, v3*, Windows, Linux, OpenVMS	CPU: Next Gen & Chipset Low voltage Itanium2 OS: HP-UX, Windows, Linux, OpenVMS DDR-II PCI-E

Timeframes not to scale

Plans subject to change

All upgrades "in-box" except as noted

New Chassis Intro. | PCI-Express | DDR-II Memory

*Not available at initial processor release

Industry CPU trends

- Shift from micro-pipelining and the frequency race to more cores per die
- Multi-threading
- Larger on-chip caches
- Increased bus frequencies, higher bandwidths, link (point to point) technologies

HP chipset futures

- Continued differentiation enabling leadership system performance
- Increases in memory bandwidth, capacity
- Improved IO and system fabric bandwidths
- Keeping up with industry standards
  - DDR-II SDRAM technology
  - PCI-Express technology
- Continued focus on reducing access latency
- Additional system reliability and resiliency features
- And more…

Tying It All Together

The Future of Computing is:

Standards-Based, Virtualized Resources, Flexible, Self-Adaptive, Multi-OS Environment, Highly Available, Utility

This future is enabled by HP

Itanium Processors / Standards Technology

▼

Leadership Systems: Leadership Performance, Price/ Performance, Resource Partitioning, Reliability, Fault Management, Availability,

▼

Multi-OS, Common Manageability

▼

Dynamic Re-allocation of Virtualized, Self-managed Data Center Resources

▼

Adaptive Enterprise

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