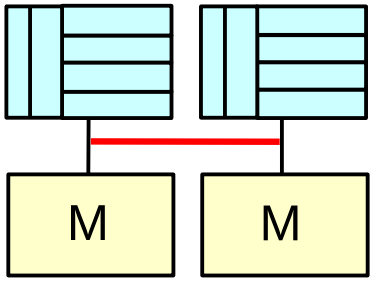
Architecting the Future - IA-64 Technology Overview

Eric Cobb

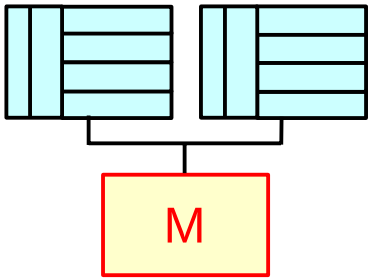
Technology Marketing Manager
Enterprise Computing Solutions Organization

Levels of Parallelism

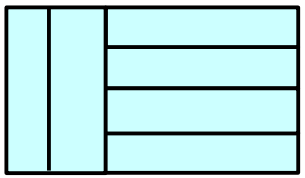
- Clusters: *Multi-Computer Systems*
  - Client-Server, Distributed Apps
  - Virtual Shared Memory Apps



- SMP: *Symmetric Multi-Processing*
  - Real Shared Memory
  - Multi-Threaded Apps
  - ccNuma straddles SMP, Clusters

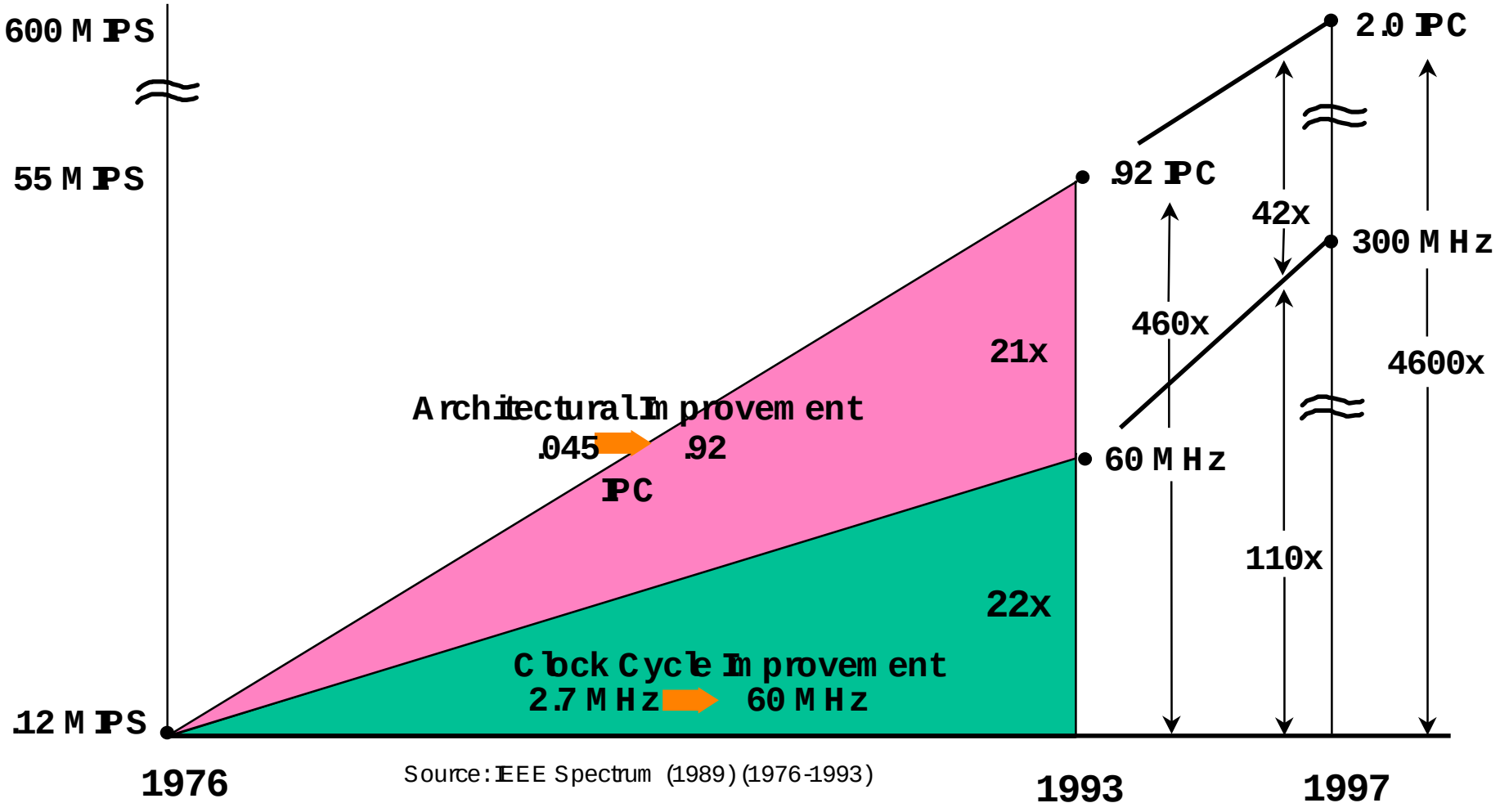


- ILP: *Instruction-Level Parallelism*
  - Pipelining, Superscalar
  - VLIW and beyond...



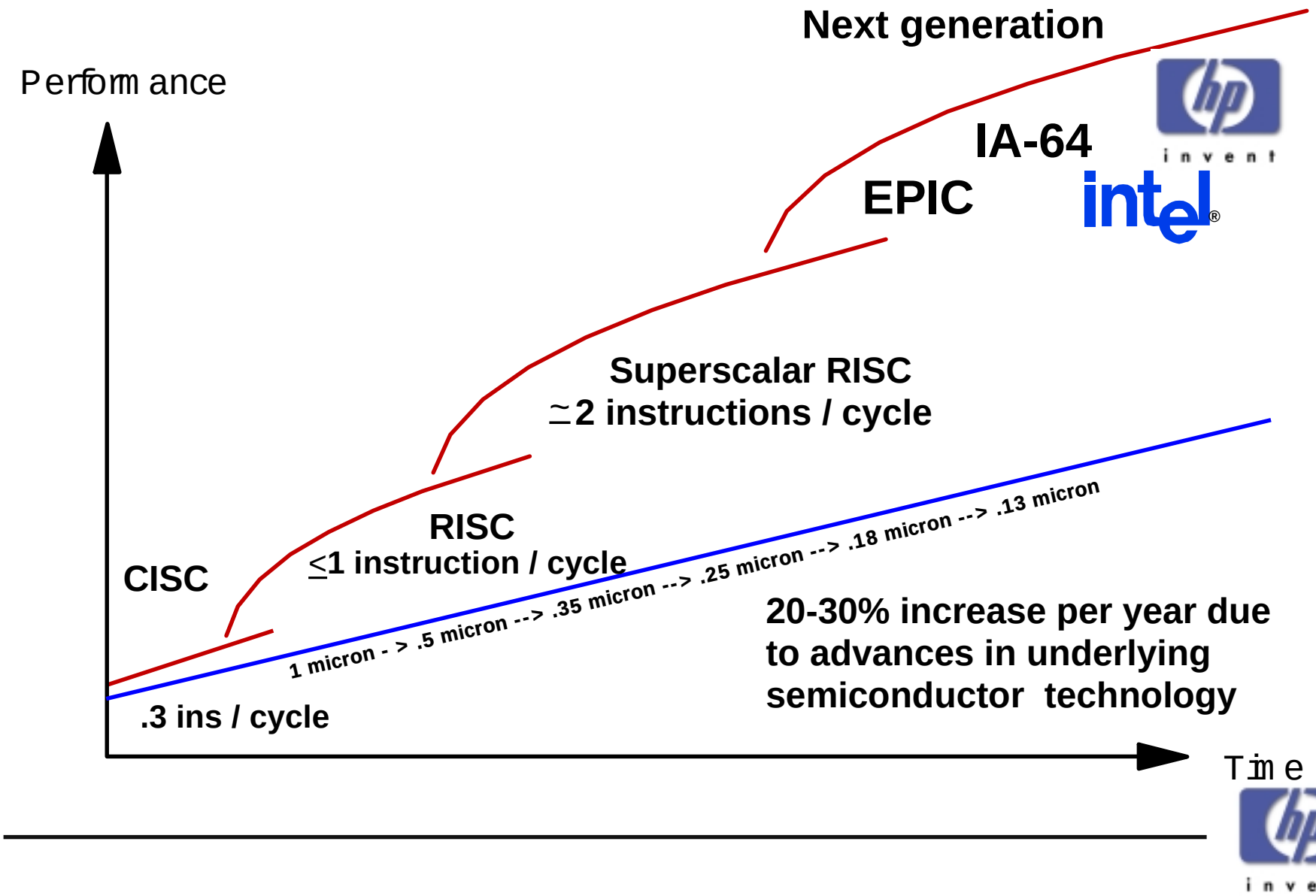
hp invent

Microprocessor Performance Growth



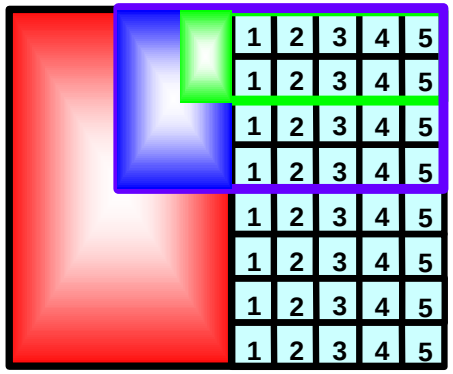
Source: IEEE Spectrum (1989) (1976-1993)

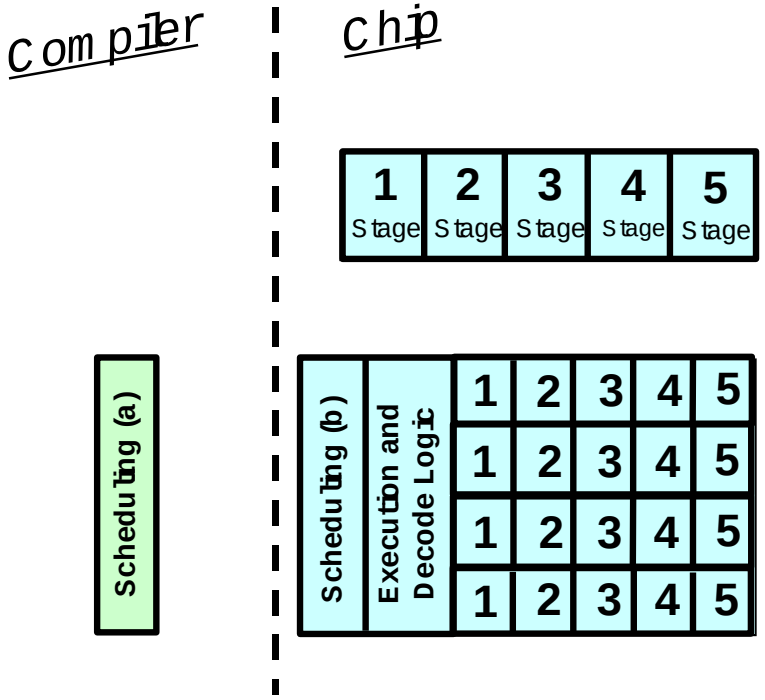
Processor Evolution



RISC Parallelism

- Pipelined Scalar RISC
  - Job broken into regular pieces
  - Pipeline stages run in parallel
- Superscalar RISC
  - Multiple parallel pipelines
  - Hardware schedules instructions and evaluates potential conflicts every cycle



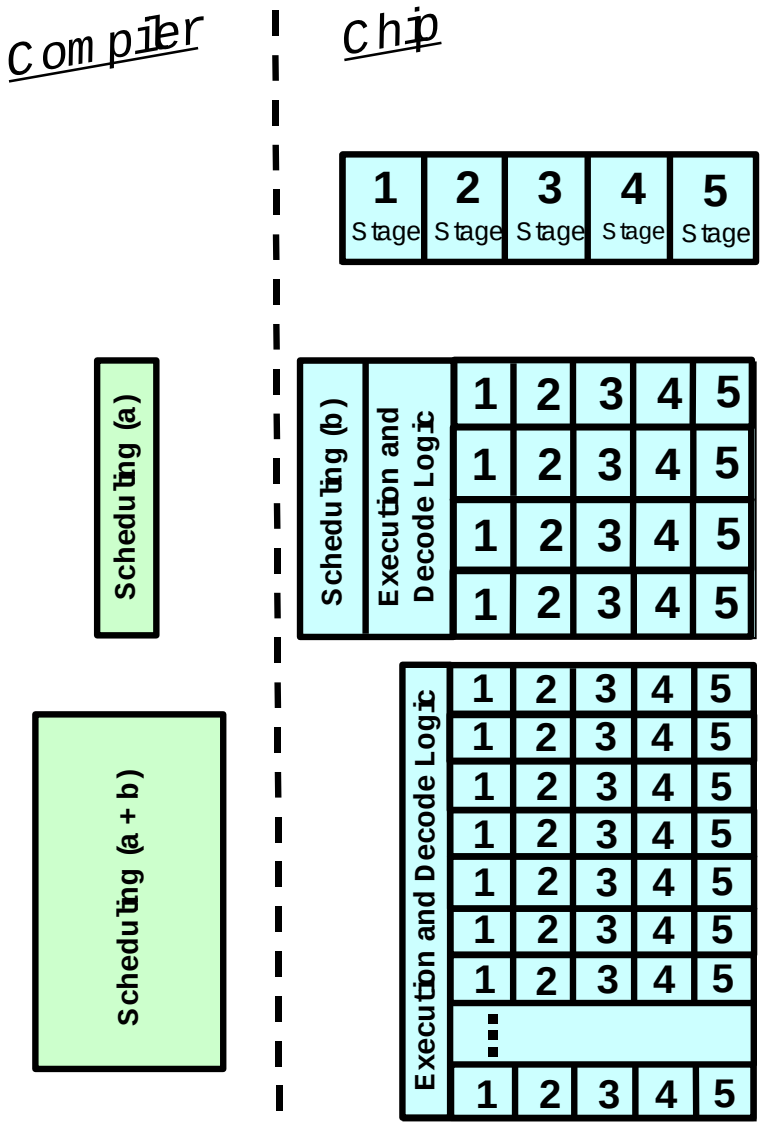


- Functional unit area grows linearly with number of units
- Scheduler area grows as the square of the number of units
- Cost-performance reaches a point of diminishing returns

hp invent

EPIC Parallelism

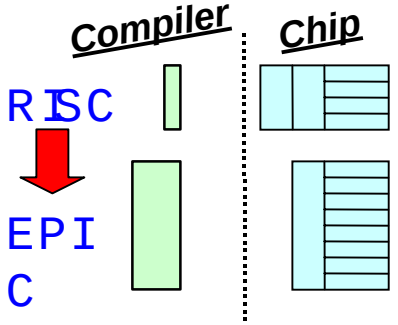
- Pipelined Scalar RISC
  - Job broken into regular pieces
  - Pipeline stages run in parallel
- Superscalar RISC
  - Multiple parallel pipelines
  - Hardware schedules instructions and evaluates potential conflicts every cycle
- EPIC (Itanium & beyond)
  - Large number of functional units
  - Compiler schedules instructions and guarantees independence



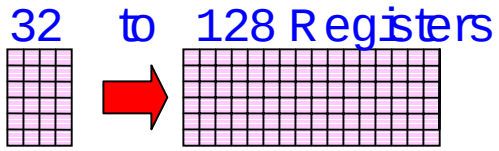
invent

Parallelism Limiters and EPIC Solution

- Complexity of multiple pipelines too great to allow effective on-chip scheduling for parallel operation
  - ➔ Solution: Explicit Parallelism (compiler handles scheduling and communicates this to the chip)

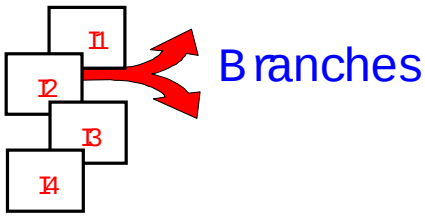


- Number of registers on chip limits parallelism
  - ➔ Solution: quadruple registers from 32 to 128 by increasing addressing from 5 bits to 7



- Large (and growing) Memory Latency
  - ➔ Solution: Speculative Loads

- Conditional and/or Unpredictable Branches
  - ➔ Solution: Prediction and Predication orchestrated by the compiler



hp invent

Industry Momentum Behind IA-64

Every major platform has made a commitment to IA-64

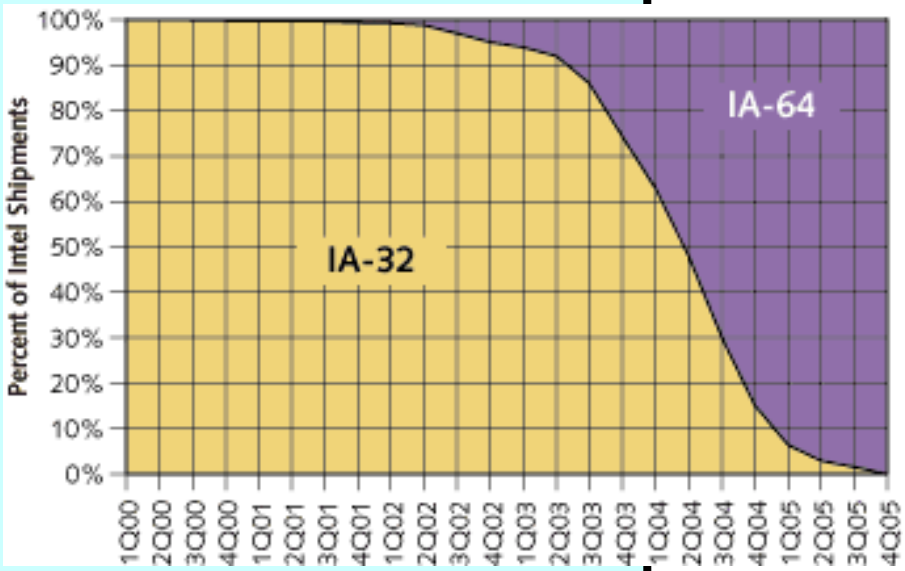
Top Microprocessor Analyst on IA-64:

IA-64 to Dominate High End

All RISCs combined can't match backing that IA-64 has today

- Dual-platform strategy is unlikely to persist once McKinley debuts in 2001
- RISCs may linger in market for years
  - SPARC and PowerPC may have enough volume to survive
  - Alpha must demonstrate superior performance for continued funding

- Linley Gwennap VP, MicroDesign Resources, November 12, 1998

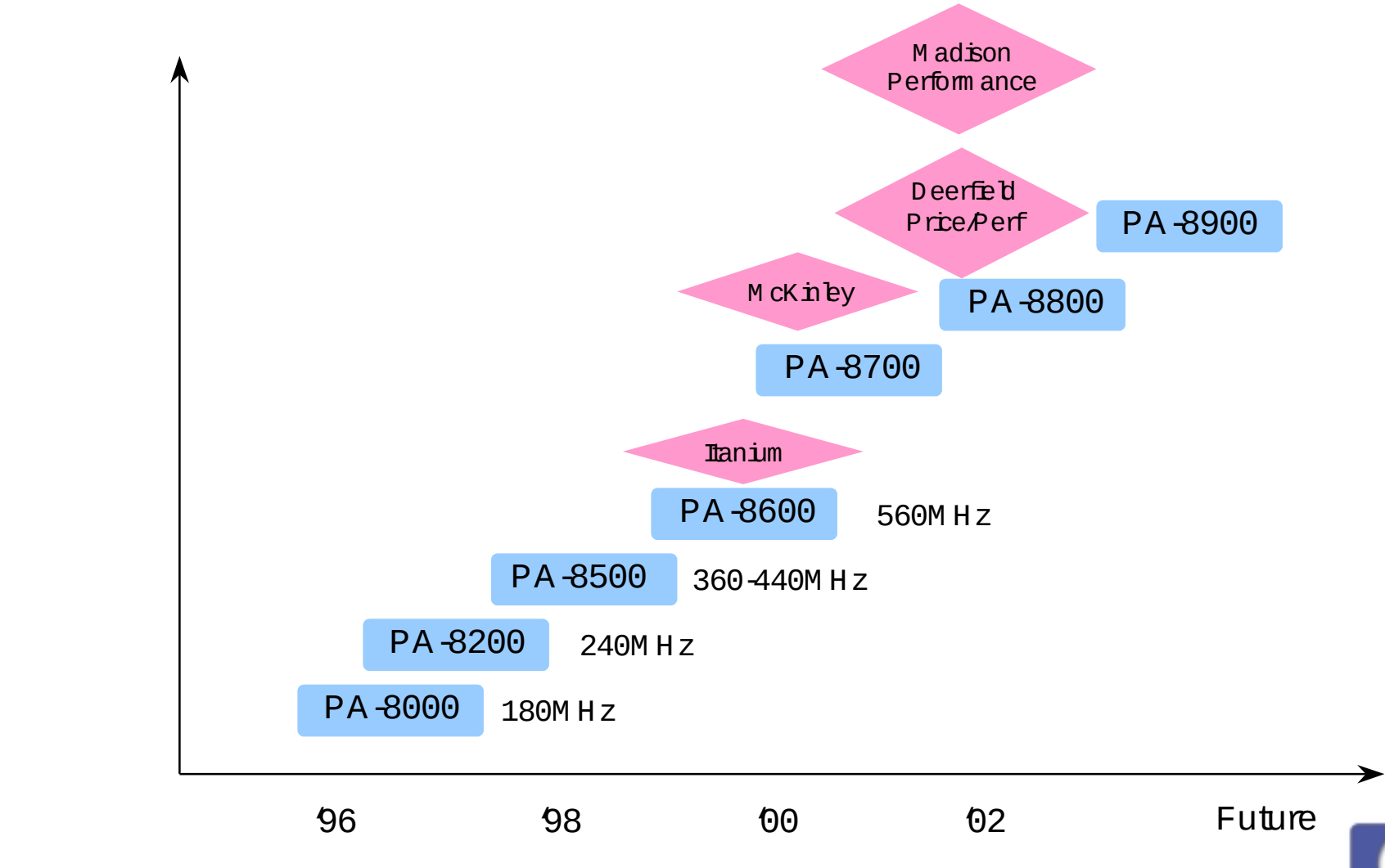


hp invent

Our Partners are Committed to IA-64

The software and Services you need when you need them !

Microprocessor Roadmap

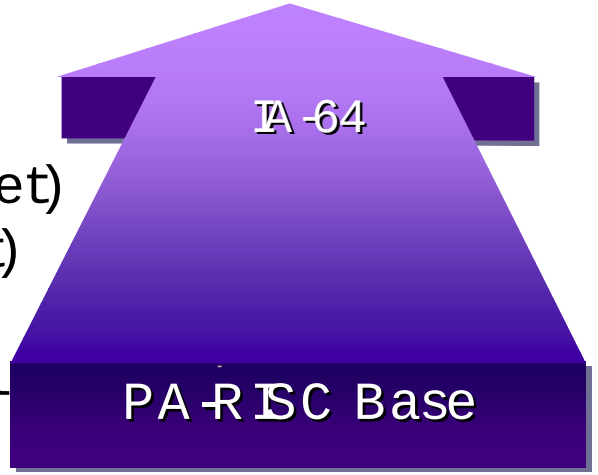


invent

PA-RISC will live on through IA-64

IA-64 retains many key PA-RISC characteristics:

- 1-to-1 mapping of performance-sensitive machine-level instructions
- PA-RISC virtual memory architecture
- Identical data formats
- PA-RISC floating point (IA-64 is a superset)
- PA-RISC multimedia (IA-64 is a superset)
- PA-RISC graphics acceleration
- Many other features still kept confidential



Benefits for PA-RISC customers:

- Smoother transition to IA-64 architecture designed in
- Easier ISV migration means more applications available sooner
- Better performance and reliability--functionality out sooner

Key: avoid "dead ends" where vendor can't move customers forward

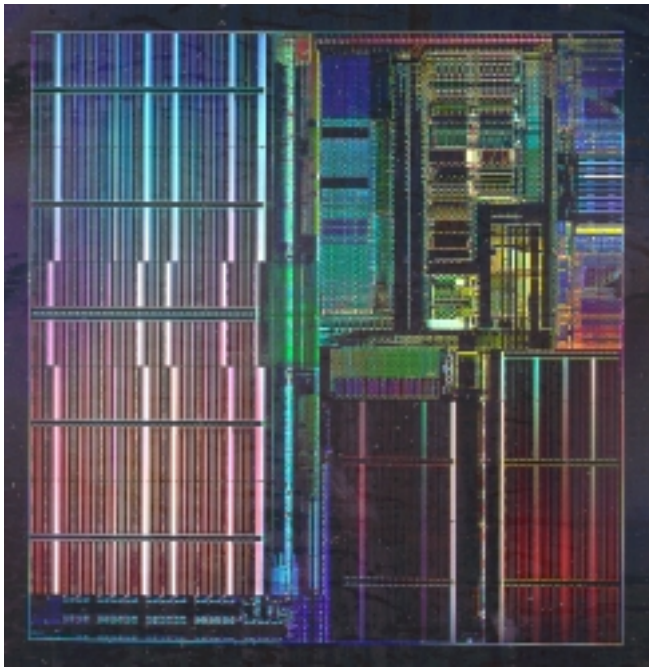
invent

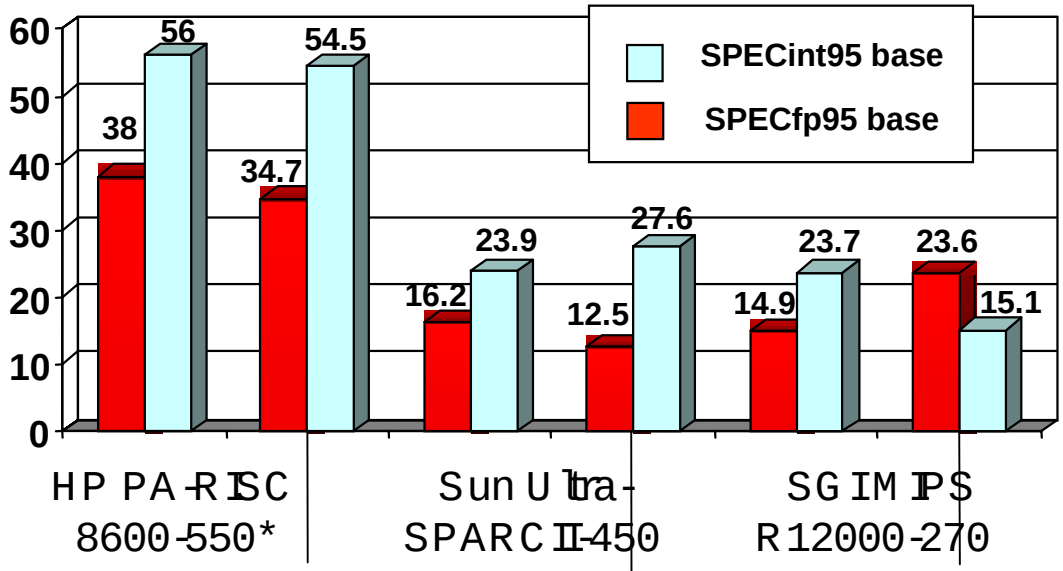
Leadership Processor Performance

- Top Integer Performance
- 1.5MB on-chip cache
- Top Floating Point Performance
- 140 Million transistors

Microprocessor Report
1998

PA-8600 Die Photo





(*) estimates

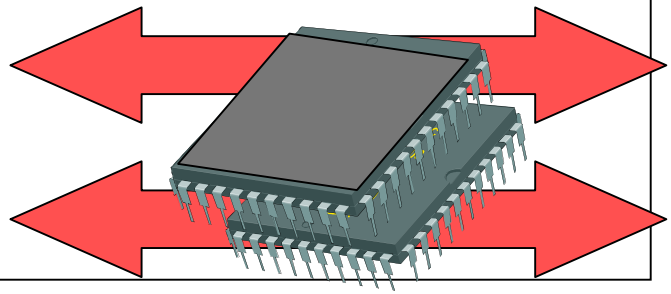
Source: HP for PA-8600 performance, SPECBENCH.ORG as of Sept. 99

invent

World's First IA-64 SMP Chipset and Bus

IA-64 system bus will be in HP's 1999 PA-RISC and IA-32 Systems and in board upgrades with IA-64 processors

- Sustained industry-leading performance
- Excellent multi-bus support and scalability
- Supports "Five 9's" High-Availability initiative
- HP-UX, MPE, NT-32 & NT-64
- PA-RISC, IA-32, IA-64
- Longevity: Investment Protection



This first IA-64 Hardware demo underscores HP's continuing commitment to IA-64 leadership

invent

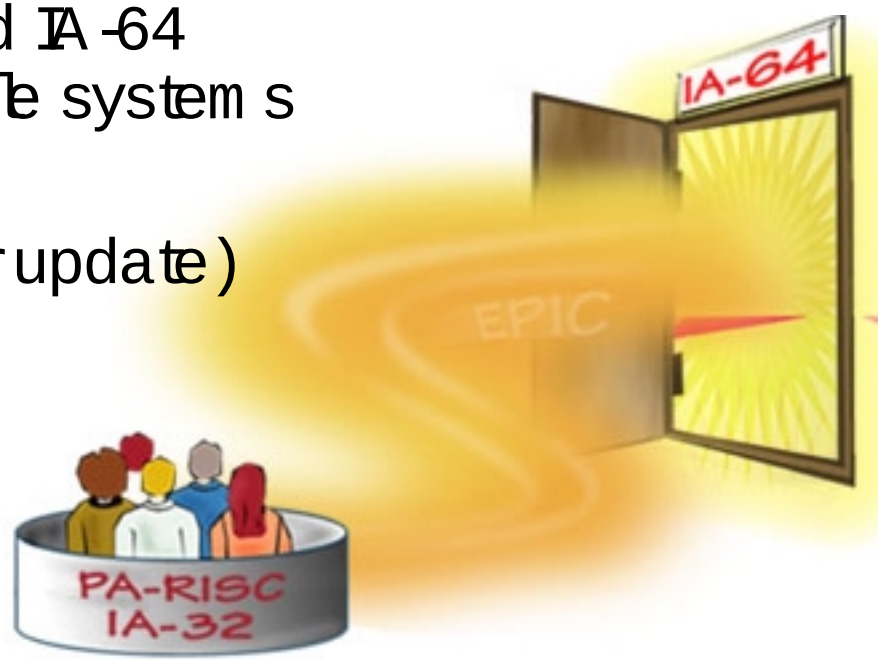
Full Binary Compatibility for PA-RISC

- Transparency:
  - Dynamic object code translator in HP-UX automatically converts PA-RISC code to native IA-64 code
  - Translated code is preserved for later reuse
- Correctness:
  - Has passed the same tests as the PA-8500
- Performance:
  - Close PA-RISC to IA-64 instruction mapping
  - Translation on average takes 1-2% of the time Native instruction execution takes 98-99%
  - Optimization done for wide instructions, predication, speculation, large register sets, etc.
  - PA-RISC optimizations carry over to IA-64

Architecting a Smooth Transition to IA-64

Hardware
- Parallel path of PA-RISC and IA-64
- IA-64-ready board upgradable systems

Operating system
- HP-UX is IA-64 ready (minor update)
- No administrator/operator interface changes
- Collaboration with Microsoft on NT transition



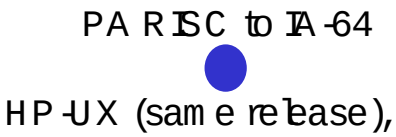
Applications
- No forced application rewrites
- No data migration
- No forced applications recompiles

invent

IA-64 Transition Plans Compared:

HP

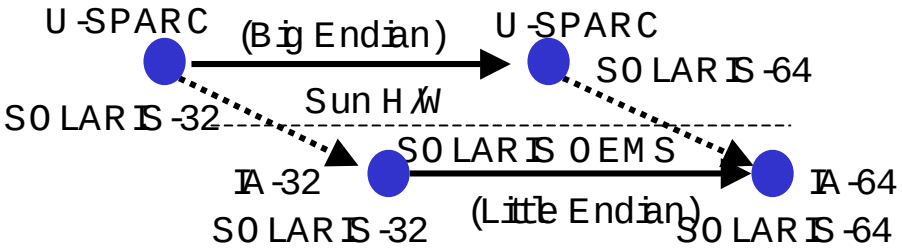
Same box, same disks. Don't even copy the data.



- Binary Compatibility: Yes
- Data Compatibility: Yes
- Board Upgrade Yes

Sun

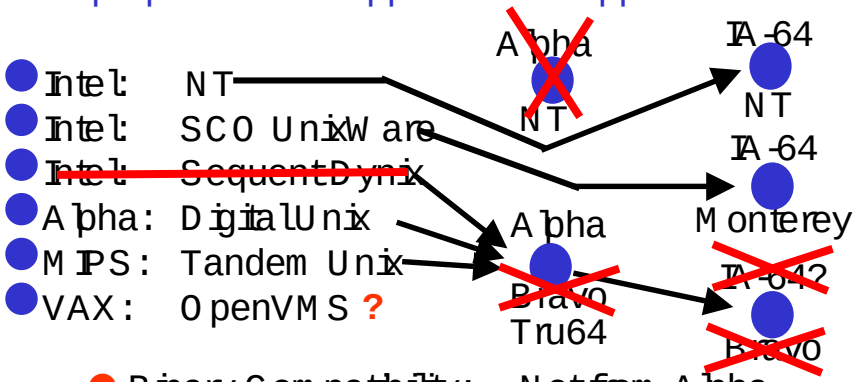
IA-32 story is OK -- big problem is SPARC to Intel transition.



- Binary Compatibility Not from SPARC
- Data Compatibility Not from SPARC
- Board Upgrade Not from SPARC

Digital/Compaq

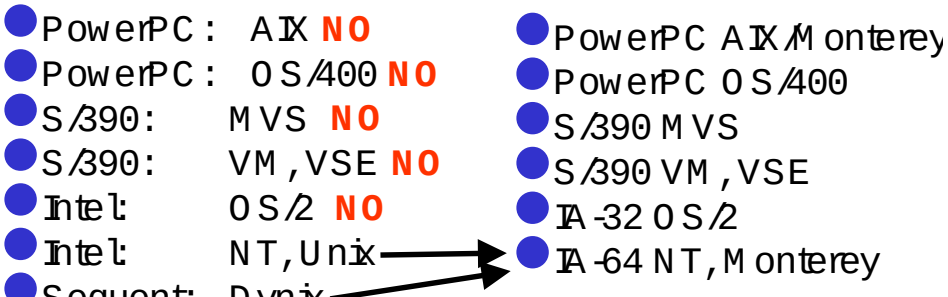
Compaq has now dropped IA-64 support from Tru64



- Binary Compatibility: Not from Alpha
- Data Compatibility: Not from Alpha
- Board Upgrade: Not from Alpha

IBM

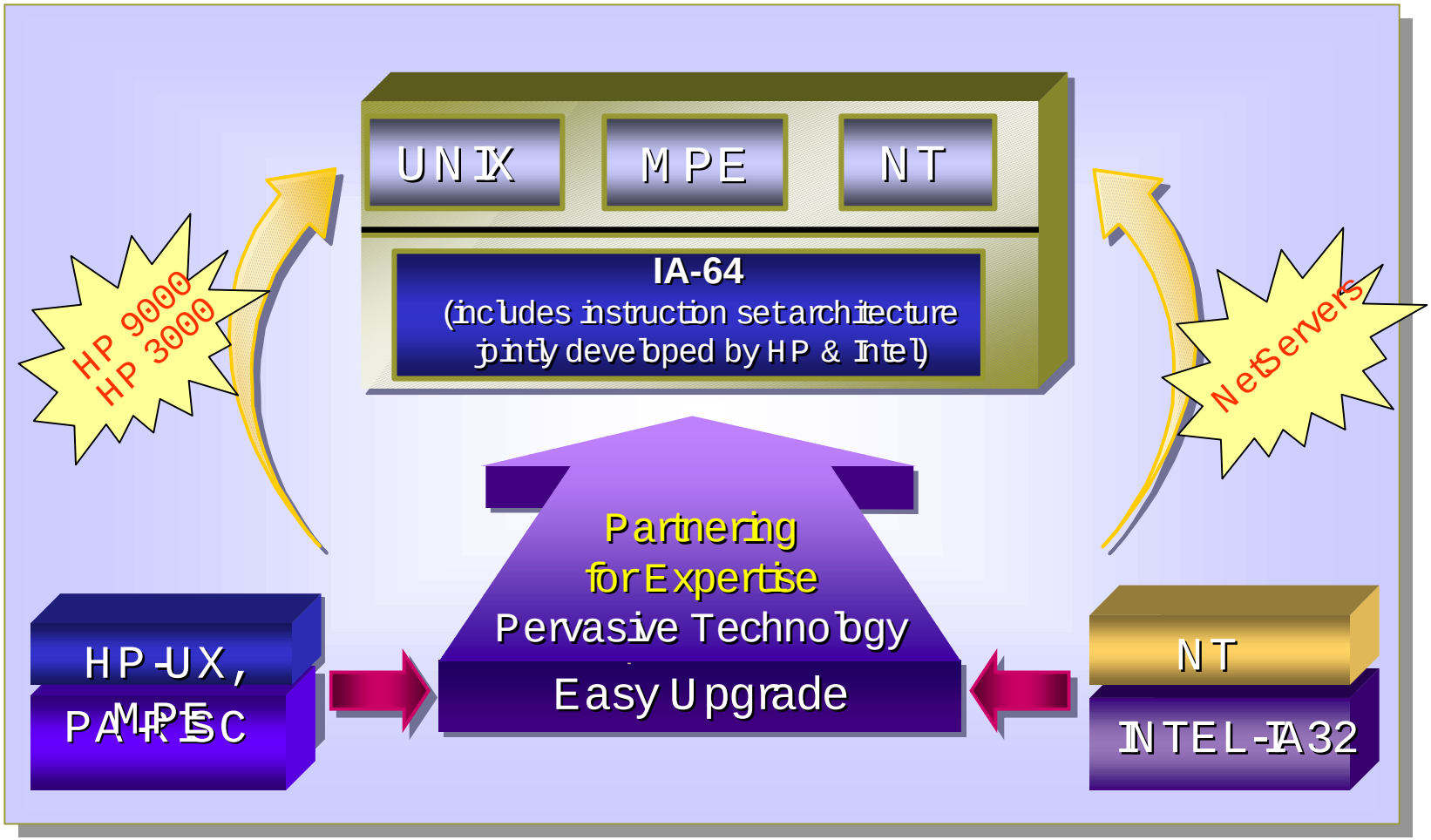
IBM's Monterey only for PC-server Unix, not RS/6000



- Binary Compatibility Not from PowerPC
- Data Compatibility: Not from PowerPC
- Board Upgrade Not from PowerPC

invent

IA-64: HP's Roadmap to the Future



invent